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Lianxi SHEN, Sung YI, Nanyang Technological University, Singapore
Jo CAERS, Xiujuan ZHAO, Kouchi (G.Q.) ZHANG, CFT/Philips, Netherlands

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Seungmin CHO, Bongtae HAN, Univercity of Maryland, USA

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Lianxi Shen, Sung Yi
School of MPE, Nanyang Technological University, Singapore, 639798
mlxshen@ntu.edu.sg, msyi@ntu.edu.sg

Jo Caers, Xiujuan Zhao, Kouchi (G.Q.) Zhang
CFT/Philips, P.O. Box 218, 5600 MD Eindhoven, The Netherlands
j.f.j.caers@philips.com

Abstract

FEM simulation for the fatigue life of CSP solder joints with various geometries and array types under thermal cycling condition is concerned in the study. Coffin-Manson law with inelastic strain range is used to estimate the fatigue life of CSP solder joints. Therefore, the two unknown material parameters in the fatigue life model need to be determined first. Actually, the two parameters are structure-dependent. In practice, they should be determined by comparing with experimental data of two typical structures so that they can characterize the fatigue behavior of other structures with common features. When determining the two structure parameters by comparing FEM results with experimental data, the criterion how to evaluate the inelastic strain range occurs. Some existing approaches include the maximum value, average values over an area or a volume around corner point. Besides the artificial factors and mesh-dependence are involved, it is found that these damage parameters don't work well for the present purpose, i.e., the predicted fatigue lives cannot be agreeable with experimental data very well. So a damage parameter based on fracture surface is proposed where the inelastic strain range is evaluated as the average value over the whole fracture surface that is near the interface between the chip-pad and solder ball. Then, the two structure parameters in the fatigue model according to Coffin-Manson law are determined by fitting with two typical experimental data. The validity of the present approach is verified by comparing with many experimental data.

Introduction

A silicon CSP with a 7×7 area array of solder joints is schematically shown in Fig. 1 a and b. The variables concerned by the present design and research include (1) the size of the pad on PCB, (2) the height of the solder joint, (3) the array type of solder joint and (4) the I/O number. The combinations of these variables are so large that it is very time-consuming to measure their fatigue life under thermal cycling condition experimentally. The more important thing is that if using experimental testing approach, the fatigue life can just known after a CSP has been designed and produced. However, if a FEM approach is properly developed, the fatigue life can be predicted in advance. This is just the purpose of the present study.

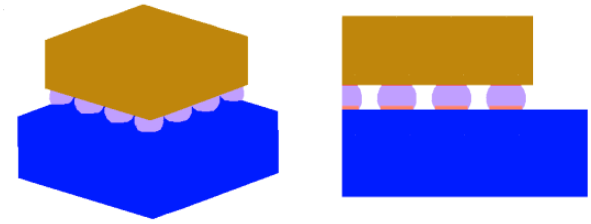


Fig. 1. Schematic diagram of chip scale package (CSP)

It is known that as various uncertain factors affect the fatigue life, it is very difficult to predict it theoretically without the help of some real experimental testing. A practical way is to modify and correlate a FEM model using some existing experimental data so that the FEM model can predict the fatigue life of new designs with reasonable accuracy.

The thermal fatigue lives for 12 different designs have been tested, which involve two solder joint geometries and 6 array types of solder joints. The different geometries of solder joint are obtained using the different substrate pad diameters and the solder volume. The experimental observation shows that fatigue raptures were always found in the solder joint and near the interface with the pad on chip. Furthermore, for the concerned designs, the diameter of the pad on chip holds the same, i.e., 280μm. These common features make it possible to develop a FEM model to predict the thermal fatigue life. In the study, six cases of the 12 experimental data are referred to correlated FEM model, while the other six are used to verify the validity of the developed FEM model.

Coffin-Manson law with inelastic strain range has extensively used as fatigue model to estimate the fatigue life of solder joints (see Yu and Shiratori, 1997; Sakai, et. al., 1999).

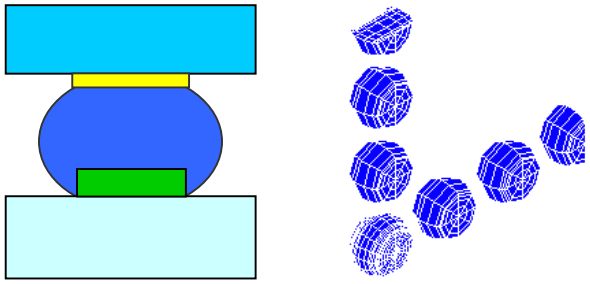
$$N_f = (\Delta\varepsilon_{in} / \varepsilon_0)^n \qquad (1)$$

where ε_0 and n are the material or structure parameters. The two unknown parameters in the fatigue life model need to be determined first. When determining them by comparing FEM results with experimental data, the criterion how to evaluate the inelastic strain range and the problem of mesh-dependence occur. The two key problem are solved by using a damage

parameter based on fracture surface where the inelastic strain range is evaluated as the average value over the whole fracture surface that is near the interface between the chip-pad and solder ball. The validity of the present approach is verified by comparing with further experimental data.

Geometries, Materials and Thermal Cycling Loading

The connection of a silicon chip to PCB through a solder joint is shown in Fig. 2 (a). The thickness of silicon chip, PCB, pad 1 (nickle pad on chip) and pad 2 (copper pad on PCB) are 680, 1000, 5 and 34μm, respectively. The diameter of pad 1 is 280μm that holds the same for all the cases. And pad 2 may be various, say 200 and 300μm in the study. The stand-off height of solder joints corresponding to the pad size 200 and 300μm are 240 and 218μm, respectively. The package with the former solder joint is called CSP11 while the latter CSP12.



(a) (b)

Fig. 2: (a) the connection of silicon chip to PCB and (b) the peripheral array of solder joints in CSP (a quarter).

The solder joint array and number at a 0.5mm pitch are shown in Fig. 2 (b). Two array types are involved, i.e., full matrix array and peripheral array, designated as M×N m or M×N p like 7×7 m or 7×7 p.

The material properties of chip, PCB (FR4), pads are treated as temperature-independent linear elastic and the corresponding properties are listed in Table 1. While the solder material is characterized as temperature-dependent visco-plastic (see Darveaux, 1988). The temperature dependent yield stress with work hardening effect is described as

$$\sigma_y = 33.9 - 0.145T + G\left(\frac{\varepsilon_{pl}}{6.1\times 10^{11}}\right)^{1/5.6} \qquad (2)$$

where σ_y, T and ε_{pl} are the yield stress in MPa, the temperature in degree Celsius and equivalent plastic strain; G is the shear modulus with G=E/[2(1+ν)]. And following Darveaux (Darveaux, 1988), the steady state creep rate is written as

$$\frac{d\varepsilon_{steady\ state}}{dt} = A_1 \frac{E}{T}[\sinh(\beta\frac{\sigma}{E})]^n \exp(\frac{-Q}{kT}) \qquad (3)$$

where A_1=6.14 (K/MPa.s)
n=3.3
β=2027
Q/k=6352 (K)
T, temperature in K

Table 1: material properties of each component in CSP

Properties	solder	Nickel Pad	Copper Pad	Chip	FR4
E (GPa)	***	200	82.74	169	25
υ	0.3	0.31	0.3	0.26	0.22
CTE (ppm/^{0}C)	25.5	13.3	16.7	2.3	16

Table 1 (Cont')

T (^{0}C)	-55	0	50	100	150	180
***	43	35.4	27.8	20.3	12.7	8

The constitutive model with isotropic flow has been implemented in the finite element code MSC MARC through user subroutine.

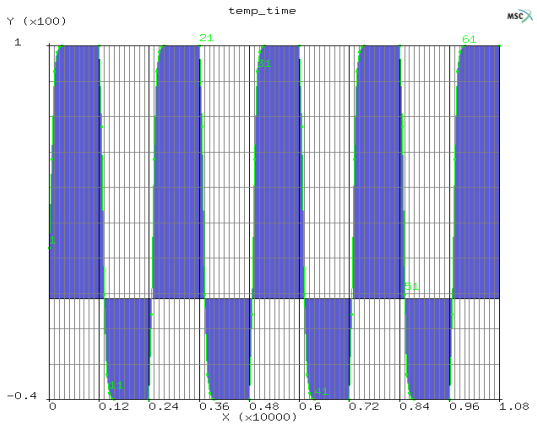
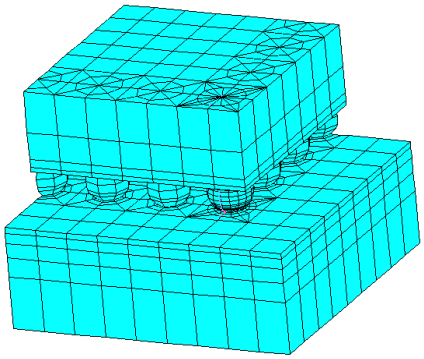


Fig. 3. Temperature history during thermal cycling.

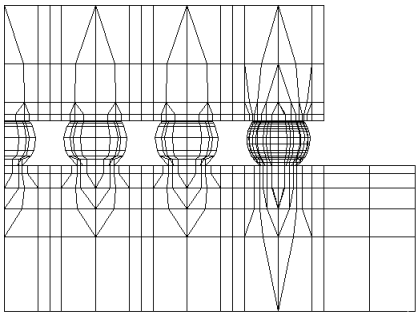
Fig. 3 shows the temperature history during thermal cycling experimental testing. The high and low temperatures are 100 and –40^{0}C, the dwell time at high and low is 14 minutes and the ramp time is 6 minutes.

Finite Element Model

Finite element method is a very useful tool to analyze the stresses and deformations distributed in a structure under thermo-mechanical loading. For the present thermal cycling loading depicted in Fig. 3, the running time of FEM code is very long due to the viscoplastic property of solder material. Therefore, it is helpful to effectively use all the elements. Fig. 4 (a) shows a three-dimensional mesh of CSP11-7×7p. A quarter is just modelled due to the symmetry. The elements of the corner solder joint are finer than others as the fatigue failure is always associated with it. It is checked that the larger PCB has no effect on the inelastic strain range of the corner solder joint. So the PCB that is a little larger than the chip are just considered in the FEM model to save elements.



(a)



(b)

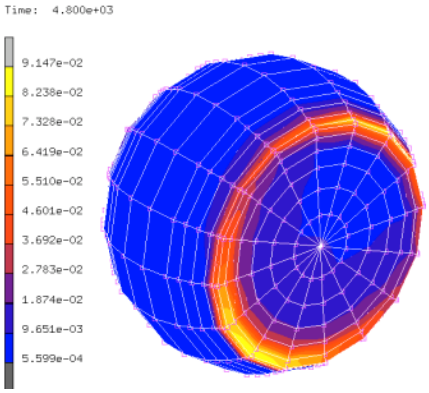
Fig. 4. Meshes for CSP11-7×7p, (a) three-dimensional one, (b) two-dimensional cross-sectional mesh.

The mesh in Fig. 4 involves 6640 hexahedral elements and 6848 nodes.

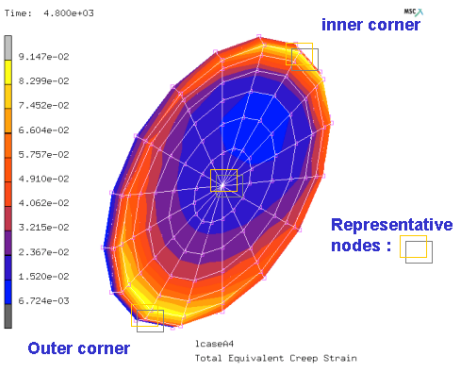
The material models for each component and thermal cycling loading described previously are inputted in FEM code MARC. The FEM solver runs for two loops in temperature history (4800s) to analyze the plastic and creep strain in the corner solder joint.

FEM Results of Inelastic Strain

The FEM simulation shows that inelastic strains concentrate around the inner and outer corners near the interface between solder joint and chip pad, as shown in Fig. 5 (a) and (b),



(a)



(b)

Fig. 5. Equivalent Inelastic strain distribution, (a) three-dimensional view, (b) cross-sectional view.

The equivalent inelastic strain distribution on fracture face under thermal cycling loading is depicted in Fig. 6. Some typical zones are marked to plot the total equivalent inelastic strain versus time for a comparison, as shown in Fig. 7. It is seen that the values in the corners are about 5 times of that in the central zone. Besides, the plastic strain is much lower than the creep strain. And it is checked that the total inelastic strain range after the second loop has been convergent. Therefore, for the 12 cases of CSP, the just two loops of thermal cycling are simulated.

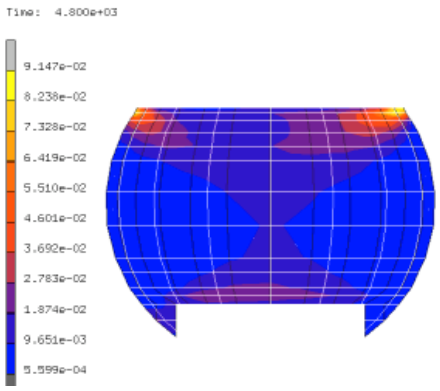


Fig. 6. Equivalent inelastic strain distribution on fracture face under thermal cycling loading.

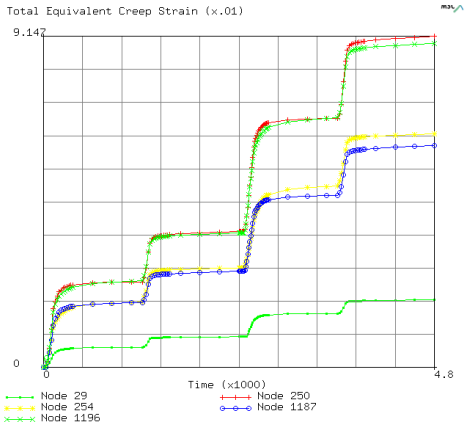


Fig. 7. The total equivalent inelastic strain versus time in two thermal cycles.

Estimation of Fatigue Life

The fatigue life model used in the study is Coffin-Manson law with inelastic strain range, which can be rewritten as

$$N_f = N_0 (\Delta \varepsilon_{in} / \varepsilon_0)^n \qquad (4)$$

where N_0 is the cycle number to failure corresponding to the inelastic strain range ε_0. FEM can determine the inelastic strain range for each node in the concerned structure. Therefore, how to select some nodes to derive the $\Delta\varepsilon_{in}$ needs to be determined first. In fact, the $\Delta\varepsilon_{in}$ characterizes the damage of solder joint during the thermal cycling. The criterion using the node with the maximum value, or average values of some nodes over an area or a volume around corner point have been used (see, Yu and Shiratori, 1999; Vandevelde et al., 2000). As shown in Fig. 8, the damage parameters based on various nodes have been checked, which include the node with the maximum inelastic strain range, the nodes in a fan zone on the fracture face and all the nodes of the fracture face. It is found that the only damage parameter based on the average inelastic strain range of all the nodes can lead to the prediction of fatigue life relatively agreeable with experimental data of 12 cases of CSP. Theoretically, the damage parameter accounts for the contribution of all the nodes on fracture face to the fatigue life. The FEM values of the damage parameter for the 12 cases of CSP are listed in Table 2. It is seen that plastic strain ranges are much lower than creep strain ranges. So the creep deformation is dominant for the fatigue failure. The inelastic strain range is obtained as the sum of the plastic and creep ones.

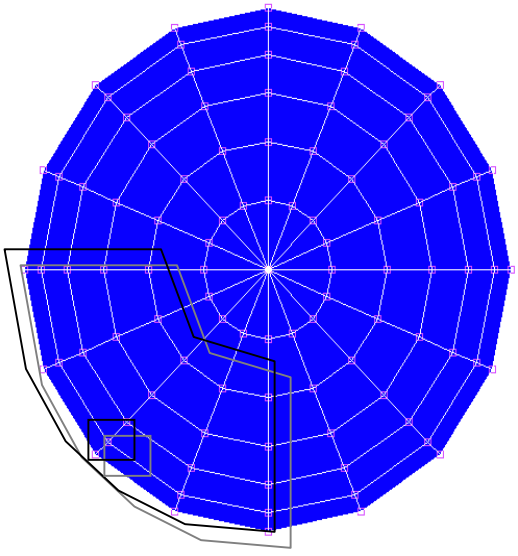


Fig. 8. Criterion based on various nodes to determine the $\Delta\varepsilon_{in}$ required in is Coffin-Manson law.

Table 2. FEM results for the damage parameter based on fracture face.

CSP types	plastic	creep	$\Delta\varepsilon_{in}$
CSP11-4×5m	0.0030	0.0154	0.0184
CSP11-5×6m	0.0033	0.0171	0.0203
CSP11-6×7m	0.0034	0.0186	0.0220
CSP11-7×7m	0.0035	0.0193	0.0228
CSP11-4×5p	0.0030	0.0156	0.0187
CSP11-7×7p	0.0038	0.0212	0.0249
CSP12-4×5m	0.0033	0.0175	0.0208
CSP12-5×6m	0.0038	0.0211	0.0249
CSP12-6×7m	0.0042	0.0238	0.0281
CSP12-7×7m	0.0044	0.0250	0.0293
CSP12-4×5p	0.0034	0.0179	0.0213
CSP12-7×7p	0.0050	0.0299	0.0349

Referring to the experimental data of CSP12-7×7m and CSP11-7×7p with blue color in Table 2, an empirical failure function is derived as

$$N_f = 575(\Delta \varepsilon_{in} / \Delta \varepsilon_0)^{-3} \qquad (5)$$

where $\Delta\varepsilon_0$=0.0249 is the inelastic strain range for CSP11-7×7p and the exponent number -3 is derived by referring to the experimental fatigue life of CSP12-7×7m.

The empirical failure function is plotted in Fig. 9 together with the experimental data of all 12 CSP types shown in Table 3. t is seen that FEM model with the empirical failure function can lead to relatively accurate prediction for the fatigue life. The slight differences between FEM prediction and experimental data for some cases are inevitable due to the randomness in experimental testing. For example, as CSP12-7×7p must be weak than CSP12-7×7m, its fatigue life should be lower than CSP12-7×7m. However, their experimental results are nearly the same.

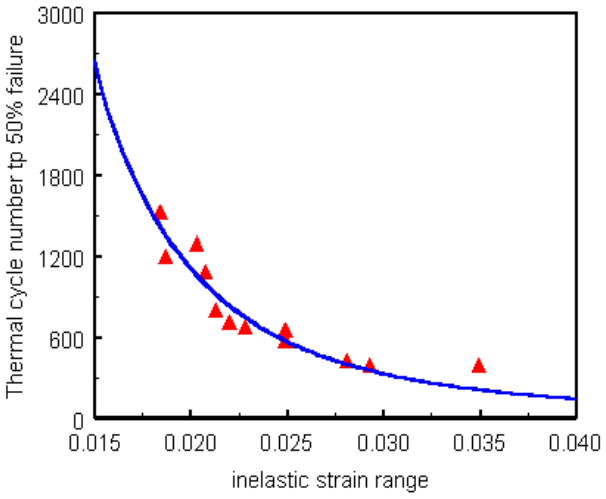


Fig. 9. Comparison between the FEM prediction and experimental data for the fatigue life of CSP.

Conclusions

As far as the fatigue life of the chip scale packages with the common feature that the chip pad size holds the same is concerned, an approach based on finite element method and an empirical failure function has been developed. The damage parameter in Coffin-Manson law with inelastic strain range is selected as the average values of all the nodes on the fatigue fracture face, which is not sensitive to the finite element mesh. Other damage parameters is not so proper for the present purpose. The prediction of the fatigue life for the typical 12 cases of CSP types confirms the validity of the present approach. Therefore, it is believed that the fatigue life for further new designs can be predicted with relatively accuracy.

References

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Electromigration Behavior of Eutectic SnPb Solder

Jae-Young Choi, Sang-Su Lee, Jong-Min Paik, Young-Chang Joo
Department of material science & engineering, Seoul National University,
San 56-1 Shilim-dong Kwanak-gu Seoul, 131-306 Korea
E-mail: adios@nownuri.net, Phone: 82-2-880-5817, Fax: 82-2-886-4156

Abstract

As the trend of miniaturization of VLSI devices, the current density of flipchip ball bumps has increased significantly and each solder joint is supporting a current density close to 10^4A/cm^2. Therefore, in SnPb eutectic solder, which have a high diffusivity at the operating temperature due to its low melting point, electromigration became a major reliability threat. We have investigated electromigration behavior of eutectic SnPb solder using thin stripe-type specimens. From the 80℃ and 100℃ testing, the activation energy for electromigration was calculated as 0.9eV and the dominant diffusion paths were through interface and surface. From the compositional analysis, it was found that Pb is a dominant migrating species than Sn atoms at 100℃ testing.

I. Introduction

As the development of integrated circuits, the number of transistors in a chip has increased very rapidly and the power consumption of the chip is also increased. The number of I/O connections that current flip chip packaging technologies provide may not fulfill the ever-increasing power requirements of giga-scale integrated circuits (GSI) or beyond. Rapid increase of the current density in flip chip led to the new reliability threat, i.e. electromigration [1].

Electromigration is a current-assisted diffusion of atoms due to a momentum transfer from electrons to the atoms in the presence of an electric field. Such a momentum transfer causes atoms to move toward the anode end, in the direction of the electron flow. The flux of atom is expressed as the product of the mobility and the net driving force as a following equation;

$$J = C\left(\frac{D}{kT}\right)Z^* q\rho j = C\left(\frac{D_o}{kT}\right)\exp\left(-\frac{E_a}{kT}\right)Z^* q\rho j \qquad (1)$$

where C is the concentration of the migrating species, D is the diffusion coefficient, k is Boltzmann's constant, Z^* is the effective charge of the atoms and it indicates the direction of atomic motion in the electric field and the effectiveness of momentum transfer from the electrons to the atoms, q is the fundamental charge, E is the electric field, ρ is the resistivity, and j is the current density[2]. Due to the electromigration, hillocks and voids are formed at the site of flux divergence, which causes depletion or accumulation of atoms. These damages can cause a failure, such as an open circuit failure in the case of void formation.

Electromigration limited reliability has been mainly studied in the chip interconnects. There is a similarity and difference in chip interconnect and flip chip bump electromigration. For example, the current density level is still low in flip chip bumps than interconnects (10^4A/cm^2 vs. 10^6A/cm^2) [1,3]. However, due to the lower melting point of the solder materials, flip chip solder has a high diffusivity at the operating temperature and it can cause a severe migration problem [3]. The geometry of flip chip bump and interconnect is quite different as well. Another big difference is its composition. Flip chip solder bump is mainly consisted of Sn and Pb. However, interconnect is mainly one materials (Al or Cu) with small amount of alloying elements. Eutectic SnPb flip chip solders have two different elements in comparable amounts. Therefore, the diffusivity of each element may be different and it may affect the electromigration reliability. Recently, the element and composition of solder are changing due to the use of lead-free solders. In that case, the electromigration characteristics of the new solder materials should be identified.

In order to study the electromigration behavior of the SnPb solder, we have fabricated thin stripe-type patterns and performed electromigration tests. Even though the stripe-type pattern has different geometry than conventional flip chip structure, it has an advantage of understanding the electromigration properties of SnPb solder, including the diffusing species and microstructure evolution. Therefore, this structure can be a good tool for characterizing solder bump material itself. We will also test the typical flip chip bump type structure to compare the electromigration performances.

II. Experimental

Figure 1. shows the SEM (Scanning Electron Microscope) image of a sample used for electromigration testing. In order to make such a structure, a bilayer Cu/Cr thin film was deposited on the oxidized Si wafer by thermal evaporation. The thickness of the Cu and Cr was 4500 Å and 500 Å, respectively. Then Cu line with 100 ㎛ width and 1000 ㎛ length was made by lithography and nitric acid etching technique. Then eutectic SnPb solder paste was dropped on the Cu line pattern after painting mildly activated resin flux. Then the sample is reflowed at 190℃ on the hot plate for 10 seconds. Then the solder was polished down until the thickness reaches about 2.5~4 ㎛ using ultrafine sand papers and 0.06 ㎛ SiO_2 emulsion on the polishing cloth. As a result,

the specimen was made up of Cr/Cu/SnPb layers which thickness was 500Å, 4500Å, 2.5~4 ㎛, respectively. The schematic diagram for fabrication procedure is shown in Figure 2.

Electromigration tests were performed on a hotplate equipped probe station. The testing temperature was 80℃ and 100℃ and the current density of the entire stripe was about 0.12MA/cm^2. However, since the stripe was consisted of copper and solder multiplayer and Cu has 1/10 of resistivity and 1/10 thickness in comparison to SnPb line, the effective current density of SnPb thin stripe pattern was approximately 0.045MA/cm^2. The resistance change of the specimen was being monitored during electromigration test.

SEM (JEOL; JSM-5600) and EDX (Energy Dispersive X-ray) were used to identify the damaging morphology and microstructure change as well as the composition changes.

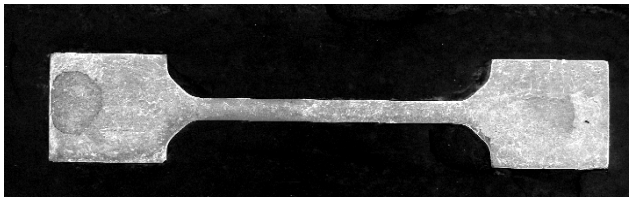

FIG. 1 SEM image of the electromigration specimen.

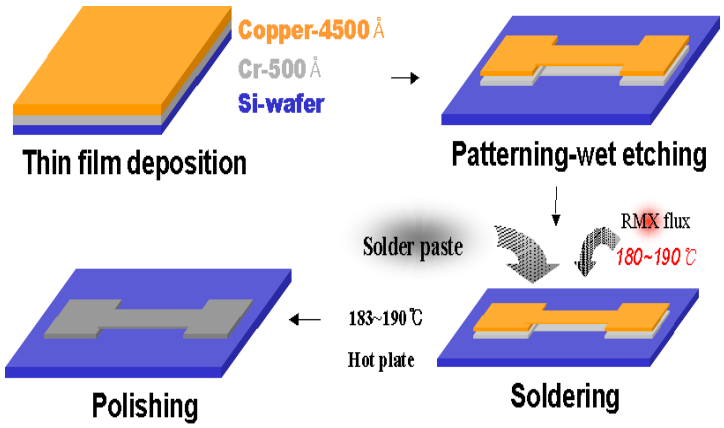

FIG. 2 Schematic diagram of sample preparation

specimen before testing and Figure 3(b) is the ones after 100℃ annealing for about 4days (without electric current stressing). Figure 3 (c) is after electromigration test at 100℃, 0.045MA/cm^2 for 4days. There is little difference between annealing (Figure 3(a) and 3(b)), but significant changes in microstructure after electromigration testing (Figure 3 (c)).

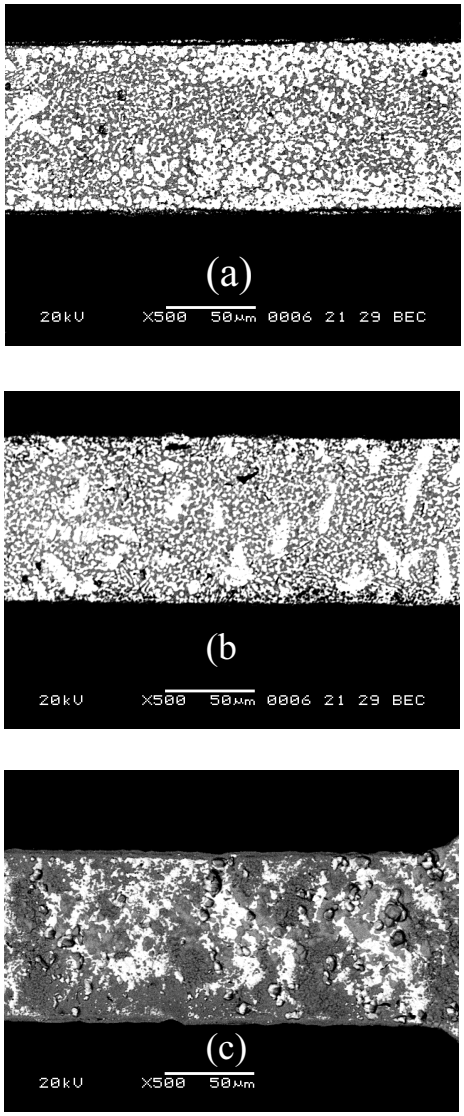

FIG. 3. BSE micrograph of the line a) before current and thermal stressing b) after 4days, 100℃ thermal stressing c) after 4days,100℃ thermal stressing and current stressing of 0.045MA/cm^2

III. Results and Discussion

A. Microstructure evolution

Figures 3 shows the SEM images of stripe EM patterns observed by BSE (Back Scattered Electron) mode. In BSE mode, the bright region is Pb-rich phase, and the dark region is Sn-rich phase. Figure 3 (a) is the SEM images of the

It was reported that the reflowed solder have two different types of microstructure depending on their cooling rate. Alternating lamellae structure with Sn-rich phase and Pb-rich phase are observed when the cooling rate is slow. If it is solidified at the sufficiently rapid cooling rate, its microstructure consists of two different phases of fine-grains [4].

In our sample, the lamellae structure is mostly observed at the pad of the specimen and the fine-grained structure is observed at the line. It is expected that the cooling rate difference in pad area and line cause the microstructure changes in line area and pad area.

When the sample was exposed to additional anneal at 100℃, white regions (Pb-rich grains) which grow like needles were observed. However, the microstructures in the two specimens do not vary widely.

After electromigration testing for 4 days at 100℃, the microstructure changes significantly as shown in Figure 3(c). At first, hillocks are observed near the anode end of SnPb stripe. But the voids are not clearly seen. Instead of the voids, the topology of line is changed. The anode side of the line is thickened, and the other side becomes thinned. And many locally depleted areas are observed as well. This may indicate that the surface or interface diffusion is dominantly occurred during electromigration than the grain boundary diffusion.

B. Resistance change induced by electromigration

Figure 4. shows the resistance change during electromigration testing at 80℃ and 100℃ under the same current density of 0.045MA/cm^2. The resistance increase during the test and the increase rate is fast at higher temperature. Interestingly there are two steps in resistance change at 100℃ testing. In the initial stage, the resistance went up rapidly, and then rate of the resistance increase slowed down after 40hours. The rate of resistance change is 1.073 %/hour for the first step and 0.255 for the second step. For 80℃, it is 0.235%/hour.

It is expected that the first part of rapid resistance increase is the microstructure and compositional change during electromigration. The second part could be the materials drift after solder have already depleted at some areas. At high temperature testing, we could observe many areas where the solder materials were already depleted after 100℃ testing.

If the first part of the resistance increase is due to the drift of the solder materials, we can compare the resistance change at two different temperatures and can acquire the activation energy of electromigration. From Equation (1), the ratio of the fluxes at two different temperatures can be written as follows.

$$\frac{J_1}{J_2} = \frac{T_2}{T_1} \exp\left(\frac{E_a}{k} \left(\frac{1}{T_2} - \frac{1}{T_1} \right) \right) \qquad (2)$$

If the resistance increase rate is proportional to the flux, then from the Equation (2), we can calculate the activation energy as 0.9eV. It is comparable with the previous reported value for activation energy of diffusion of Pb or Sn[5].

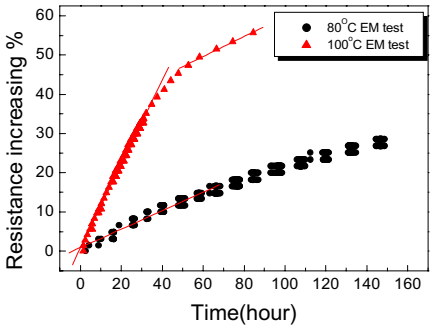

FIG 4. Time-resistance curves under thermal and current stressing

C. Dominant Diffusing Element

Electromigration is a current-assisted diffusion of atoms due to a momentum transfer from electrons to the atoms in the presence of an electric field. Therefore, Pb and Sn are forced to migrate toward the anode end, which is the direction of electron flow, which is the direction of electron flow [2]. However, diffusivities and effective charges are different to each other and one element may move faster than the other element at specific temperature and current density. Identifying such an element is important in understanding electromigration-induced failure mechanism.

We have studied the compositional change of cathode side and anode side of the lines using BSE, EDS (Energy Dispersive Spectrometer), and EDX mapping.

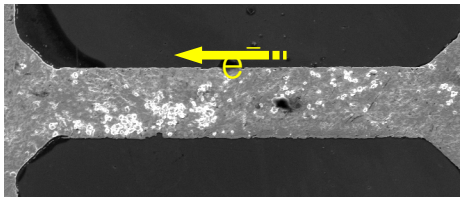

FIG. 5. SEM image of the specimen 80℃ thermal stressing and the current stressing of 0.045MA/cm^2 for 6days

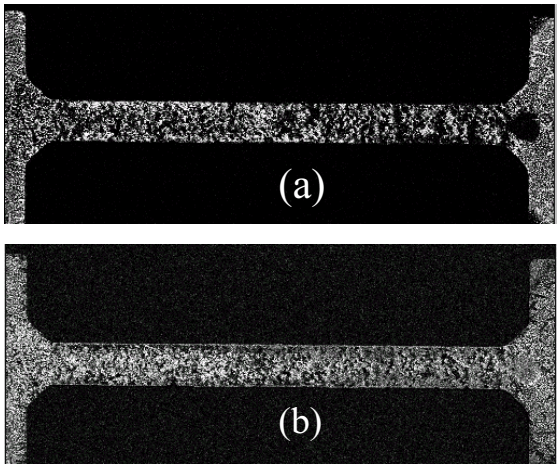

FIG. 6. EDX maps of (a) Pb and (b) Sn atoms in the specimen tested at 100℃, under the current density of 0.045MA/cm^2 for 4days

For conventional SEM observation by SE(Second Electorn) detector, we could confirm that hillocks were accumulated at the anode end of the line at 80℃, 0.045MA/cm^2 testing as shown in Figure 5. Interestingly this trend is less clear for 100℃, 0.045MA/cm^2 sample.

Figure 6. shows the EDX mapping results in the 100℃, 0.045MA/cm^2 tested sample. The Pb mapping shows more white dots in anode end of the line, which indicates that Pb atoms accumulated at anode end. However, for Sn atoms, it was difficult to identify the migration of Sn atoms. EDX composition analysis also showed that more Pb atoms migrated more than Sn atoms.

In the case of the BSE, observation results are shown in Figure 7. In BSE mode, Pb-rich grains are shown as a bright area and Sn-rich grain is a dark area. In Figure 7, we can see that there is far more bright area in anode end of the line than the cathode side. Therefore, there are more Pb atoms in the anode end of the lines.

After taking all the EDS, BSE, EDX mapping data into consideration, we can say that Pb atoms moves faster than Sn during electromigration at 100℃. Our line is connected with relatively large pad area, so we could not exclude the effect of pad, which can act as a source or sink of atoms. However, the general trend of our observation that Pb atoms migrated faster than Sn atoms should hold for 100℃ testing. Tu *et al*. have reported that Pb migrated atoms migrated in the flip chip type test structre tested at 100℃ [5]. His group also report that at room temperature testing, Sn atoms are dominat migrating species. This indicates that diminate diffusing species varies with temperature.

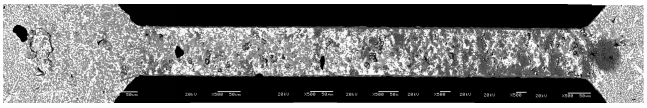

FIG. 7. BSE micrograph of the specimen after electromigration at 100℃ under 0.045MA/cm^2 current density for 4days.

IV. Conclusion

Electromigration characteristics of eutectic SnPb solder has been investigated using thin stripe-type specimens. The electromigration testing results at the temperature of 80℃ and 100℃ and under the current density of 0.045MA/cm^2 showed that;

1. Hillocks were observed at the anode end, but voids were not clearly observed in cathode end. Instead, the thickness of the stripe at the cathode end was decreased and many locally depleted regions were observed there. It indicates that surface or interface diffusion is more dominant than the grain boundary diffusion.
2. From the resistance change at 80℃ and 100℃, the activation energy is calculated as 0.9 eV.
3. BSE, EDX, and EDS analysis showed that the dominant diffusing species at 100℃ is Pb atoms.

V. Acknowledgments

This work was supported by Center for Electronic Packaging Materials of Korea Science and Engineering Foundation.

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Thermo-mechanical and Flexural Behavior of WB-PBGA Package Using Moiré Interferometry

Jinwon Joo[1], Kihwan Oh[1], Seungmin Cho[2] and Bongtae Han[2]

[1]Department of Mechanical Engineering
Chungbuk National University
Cheongju Chungbuk, 361-763 Korea
jinwon@cbucc.chungbuk.ac.kr

[2]CALCE Electronic Products and Systems Center
Department of Mechanical Engineering
University of Maryland,
College Park, MD 20742, USA

Abstract

Thermo-mechanical and flexural behavior of a wire-bond plastic ball grid array (WB_PBGA) package assembly is characterized using high-sensitivity moiré interferometry. Using the real-time moiré setup, fringe patterns are recorded and analyzed at several bending loads and temperatures. Detailed global and local deformations of the assembly are investigated. The deformations caused by thermally induced bending were compared with those caused by mechanical bending. The results reveal highly nonlinear behavior of the package assembly under thermal loading. The sign (direction) of the shear strain caused by the mechanical bending was the opposite of that caused by the thermal load. The results also show that real-time moiré interferometry is a powerful and effective tool in experimental studies of electronic packaging.

Introduction

An increased use of chip carriers with many small leads, such as the plastic ball grid array (PBGA) package, has been reported in recent years. Investigation on failures in solder interconnections becomes more important for reliability assessment of microelectronics. An electronic package assembly comprises various materials that have different thermo-mechanical properties. The nonuniform properties of the silicon die, the molding compound and the printed circuit board (PCB) produce variations in strain within the PBGA package assembly, which is subjected to cyclic thermal and/or mechanical loading. As portable electronic products are reduced in size, especially in thickness, isothermal flexural fatigue as well as thermal cycling fatigue becomes important reliability issues. An understanding of the thermal and mechanical response of the various components is critical for improving package design and yielding maximum performance and reliability.

The accelerated thermal cycling test (ACT), in which electronic assemblies are cycled through extremes of temperature, has been used extensively [1,2] for assessing thermal fatigue. The measured fatigue life is useful for comparing designs, but provides only limited information about the thermo-mechanical response. The nonlinear behavior, such as the plastic deformation and creep of solder, makes it more difficult to determine the conditions of the ACT, and thus to predict the reliability of electronic devices. Finite element analysis can be used [3,4] to estimate deformations and stresses in electronic package assemblies. While the finite element method is a useful numerical tool for detailed prediction of stresses and strains in almost every kind of package with any loading condition, the models and results usually require precise experimental verification.

Moiré interferometry is a full-field optical method that provides high-sensitivity displacement measurement and high spatial resolution [5]. Recently, the applicability of the method has been extended to thermal deformation analysis of microelectronics devices [6-10]. Most previous studies of PBGA packaging reliability, however, focus on the effect of thermal cycling or bi-thermal loading. Only a few recent studies [11,12] address any type of mechanically induced deformation in BGA packages. In this paper, thermo-mechanical and flexural behavior of a wire-bond plastic ball grid array (WB-PBGA) package assembly is characterized by high-sensitivity moiré interferometry. Using the real-time moiré setup, fringe patterns are recorded and analyzed for several bending loads and temperatures. Detailed global and local deformations of the assembly by thermal and mechanical loadings are investigated. The deformation caused by thermally induced bending is compared with that caused by mechanical bending.

Background: Real-Time Moiré Interferometry

Moiré interferometry is an optical measurement method providing whole-field contour maps of in-plane displacements with a subwavelength sensitivity. In moiré interferometry, a high-frequency (usually, 1200 lines/mm) crossed-line diffraction grating is replicated on the surface of the specimen and it deforms together with the underlying specimen. The deformed specimen grating interacts with a reference grating to produce the moiré fringe pattern. The resulting fringe patterns represent contours of constant U and V displacement fields, defined as in-plane displacements in orthogonal x and y directions, respectively. The displacements are determined from the fringe orders by

$$U = \frac{1}{2f_s} N_x \ , \quad V = \frac{1}{2f_s} N_y \tag{1}$$

where N_x and N_y are fringe orders in the U and V field patterns, respectively. In routine practice, a virtual reference grating with a frequency f of 2400 lines/mm is used, which provides a displacement sensitivity of 0.417 μm per fringe order.

In cases where the strains are calculated from the measured displacement fields, they are determined by the small-strain relationships

$$\varepsilon_x = \frac{\partial U}{\partial x} \approx \frac{1}{2f_s}\left(\frac{\Delta N_x}{\Delta x}\right), \quad \varepsilon_y = \frac{\partial V}{\partial y} \approx \frac{1}{2f_s}\left(\frac{\Delta N_y}{\Delta y}\right)$$

$$\gamma_{xy} = \frac{\partial V}{\partial x} + \frac{\partial V}{\partial x} \approx \frac{1}{2 f_s}\left(\frac{\Delta N_y}{\Delta x} + \frac{\Delta N_x}{\Delta y}\right) \quad (2)$$

Real-time moiré interferometry [13] is capable of documenting thermally induced deformations as a function of temperature and time with sub-micron displacement sensitivity. For real-time measurement, a compact moiré interferometry system and environmental chamber were utilized in this experiment. Vibrations caused by the chamber usually produce relative motions of the specimen and/or optical elements. To prevent inadvertent vibrations, the specimen is mechanically isolated from the chamber by a specimen holder connected only to the moiré system.

Experimental Procedure and Fringe Patterns

Specimen

The package assembly used in the experiment was a 27 mm WB-PBGA package with 225 I/Os (15 x 15 solder interconnection array) mounted on an FR-4 PCB with eutectic solder balls. The specimen, with a strip array configuration, was prepared from the assembly, containing several central rows of solder interconnections. A cross-section of the WB-PBGA package assembly is shown in Fig. 1 with relevant dimensions. The solder balls were 0.97 mm high and the largest diameter was 1.10 mm. The pitch between solder balls was 1.50 mm.

One side of the specimen was ground flat to expose the largest cross-section of the solder balls and was polished with a 5 μm diamond paste. The specimen was maintained at 80°C in the environmental chamber for about 2 hours before specimen grating replication to ensure the exclusion of any existing moisture from the assembly. A high-frequency (1200 lines/mm) crossed-line diffraction grating was replicated on the surface of the specimen at room temperature (20°C).

Mechanical loading

A bending test apparatus was designed for use in conjunction with a compact moiré interferometer to test the effect of bending on electronic package assemblies and other small components. As shown in Fig. 2, the tester consists of two wedge blocks, an electrical loadcell, upper and lower four-point bending fixtures, two driving screws and a frame body. The compressive displacements are achieved by driving the lower wedge to the left.

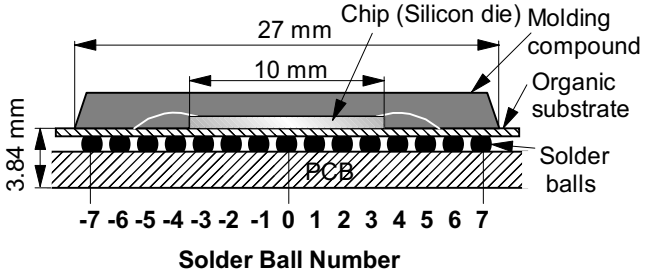

Fig. 1 Schematic diagram of a sectioned WB-PBGA package assembly

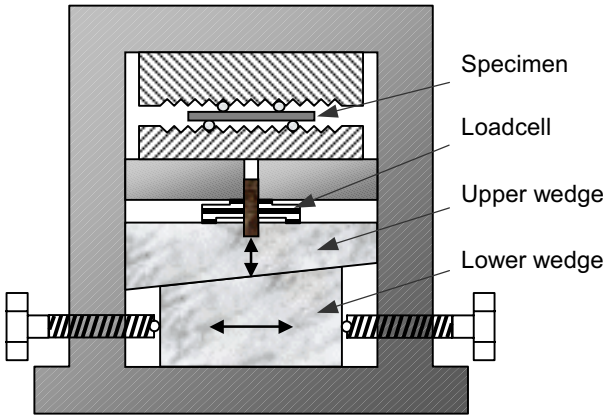

Fig. 2 Schematics of four-point bending fixtures

The specimen with undeformed grating was placed at the edge of the fixtures so that the incoming laser beams were not blocked. Bending tests were performed with the upper bending fixture placed on the top of the chip carriers so that the loading pins were situated between solder ball numbers -7 and -6, and between numbers 6 and 7, as shown in Fig. 3. Teflon tape was wound around the pins to minimize friction between the fixture, the pins and the specimen. A compact four-beam moiré interferometer (PEMI II, Photomechanics, Inc.) was used in the test. By rotation of the interferometer instead of the specimen, the specimen grating was aligned with the virtual reference grating and the initial null field was obtained. This zeroes the optical system and ensures that the fringes measured later are pure load-induced fringes. The package assembly was tested under applied loads ranging from 0 to 22.2 N. Moiré fringes were recorded at the resulting pure bending moments of 14.1 N.m, 21.2 N.m, 28.2 N.m, 35.3 N.m, 42.3 N.m, 56.4 N.m and 70.6 N.m. The specimen was then unloaded, and fringes were recorded at the moments of 35.3 N.m and 0 N.m.

The representative fringe patterns obtained at 28.2 N.m, 42.3 N.m, 70.6 N.m and 0 N.m (unloading) are shown in Fig. 4. The applied bending moment causes compressive strains in the region of the molding compound, and tensile strains in the region of the PCB. The hyperbolic patterns of the U field are

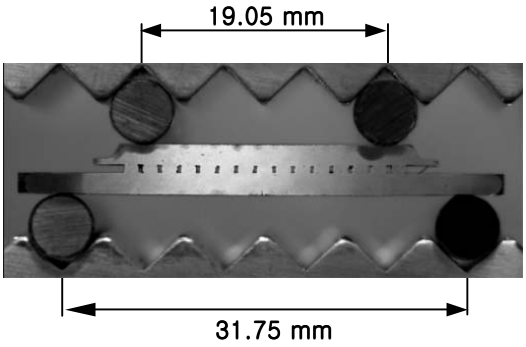

Fig. 3 Four-point bending test of WB-PBGA package assembly with moiré grating

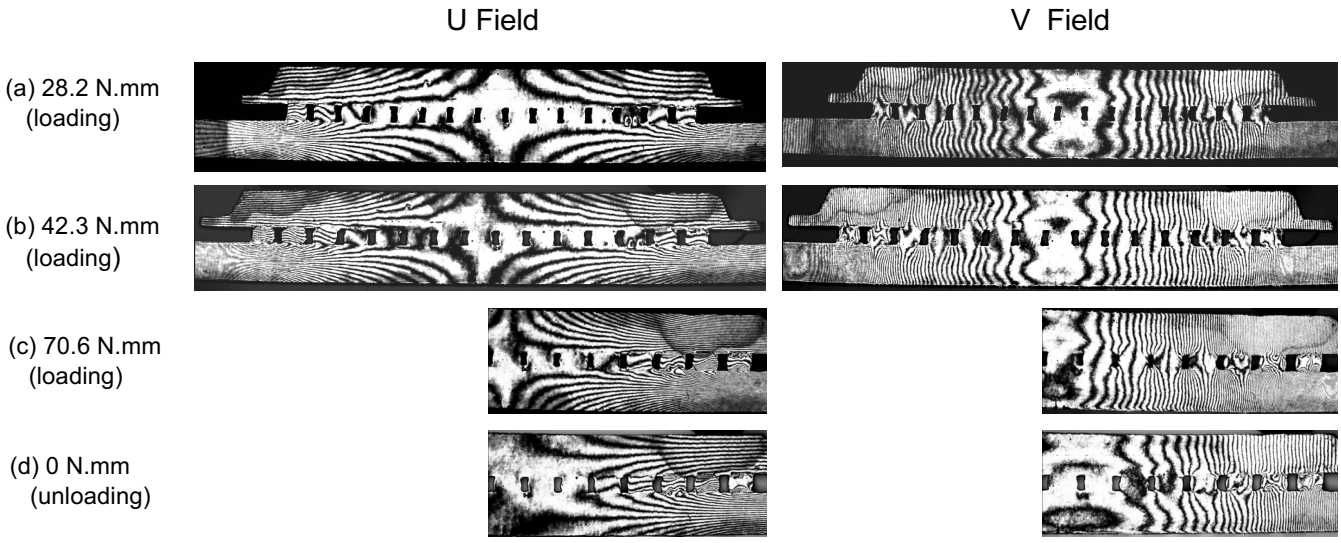

Fig. 4 Fringe patterns of the WB-PBGA package assembly in four-point bending

similar to those of an isotropic beam subjected to bending. The bending strain $\partial U/\partial x$ is nearly zero in the region of the chip because of its high stiffness. At higher moments, the normal strains $\partial U/\partial x$ and $\partial V/\partial y$ are nearly zero in the central solder balls. However, outlying solder balls experienced shear strains of considerable magnitude, as can be seen from the concentrated fringes in the U displacement field. The fringe pattern at the moment of 0 N.m (unloading) shows that the mechanical loading cycle produced a permanent bending deformation and a localized shear strain in the solder balls at each end.

Thermal loading

Real-time moiré interferometry was conducted for the measurement of in-plane displacements produced by the temperature changes. Figure 5 depicts the temperature profile used in the thermal loading experiment. The same specimen used in the mechanical bending test was prepared and installed in the environmental chamber at room temperature. The specimen was then heated and subjected to one thermal cycle. The maximum and minimum temperatures were 125°C and -40°C, respectively. The fringe patterns were recorded at several points within the temperature range.

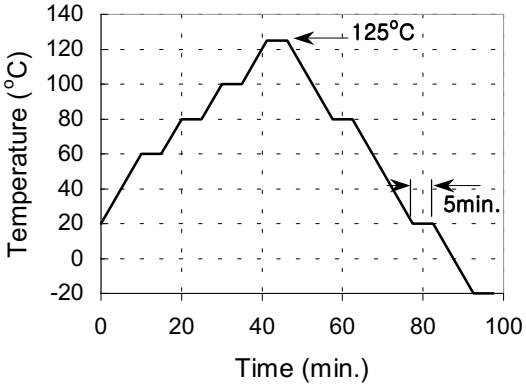

Fig. 5 Temperature profiles used in the experiment with thermal loading

The representative fringe patterns obtained at 80°C (heating), 125°C (heating), 80°C (cooling) and -20°C (cooling) during thermal loading are shown in Fig. 3. The fringe patterns induced by temperature change were quite different from those induced by mechanical bending, while apparent bending shapes appeared to be similar. The difference was ascribed to the superposition of thermal expansion in all directions onto the global bending caused by the mismatch of coefficients of thermal expansion (CTE). The difference between the fringes at 80°C (heating) and 80°C (cooling) highlight the temperature-dependent nonlinear behavior of a WB-PBGA package assembly. It is interesting to note that the fringe patterns at 80°C (heating) and -20°C (cooling) seemed to be similar, which indicates that temperature-dependent nonlinear deformation was much less significant during the cooling process.

Results and Discussion

Flexural Behavior

The bending displacements (V displacements) subjected to mechanical bending along the centerline of the package were determined by Eq. (1), and the results obtained for the right half of the package are plotted in Fig. 7. The bending displacement increased linearly as the bending moment increased to the moment of 42.3 N.m. However, the bending displacement in the region outside the chip area increased at a much higher rate when the moment increased further to 70.6 N.m. As in the case of plastic deformation of a typical metal, the bending decreased linearly when the moment decreased to zero. As a result, the loading cycle produced a significant amount of permanent bending

The longitudinal strain, ε_x, along the top of the molding compound was determined by Eq. (2), and the results are plotted in Fig. 8. The mechanical bending resulted in compressive strain on the top surface of the molding compound. The chip extended from -5 mm to 5 mm (dashed lines in the graph) under the surface of the molding compound.

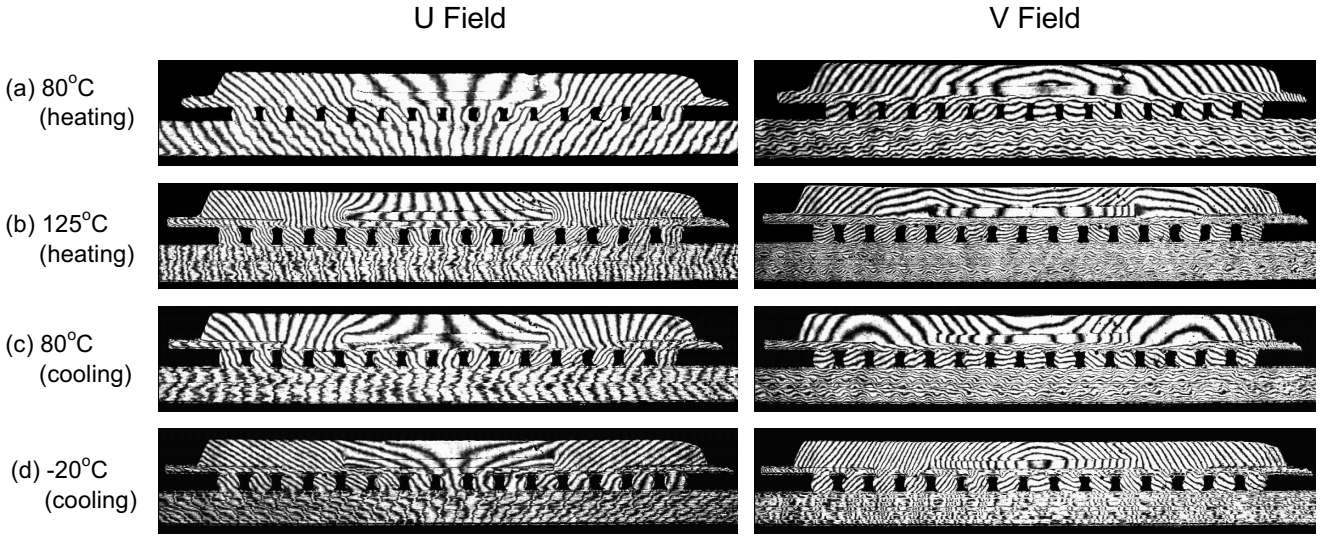

Fig. 6 Fringe patterns of the WB-PBGA package assembly caused by temperature change

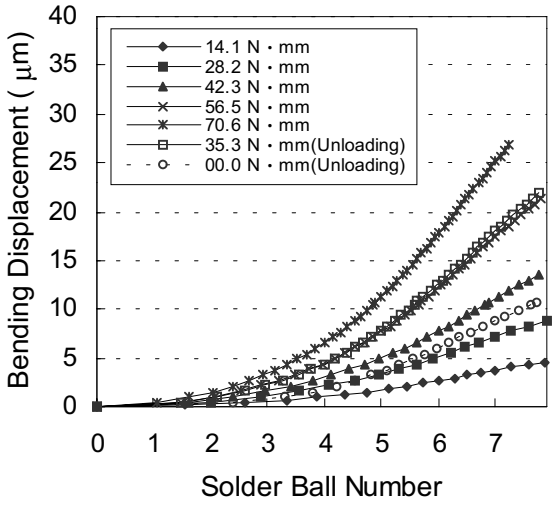

Fig. 7 Bending displacement distributions in the four-point bending

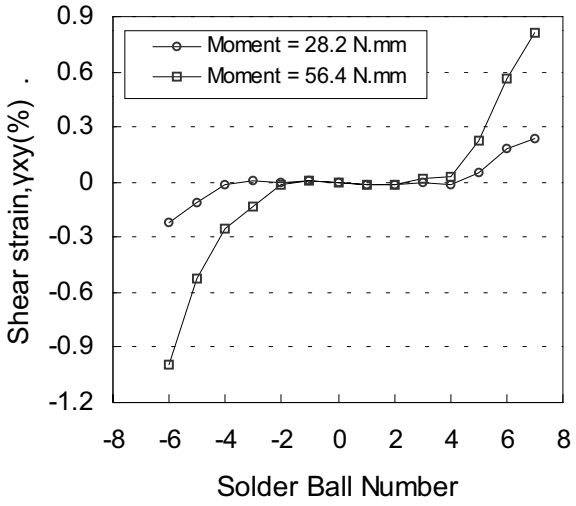

Fig. 9 Average shear strain distributions for WB-PBGA solder balls in the four-point bending

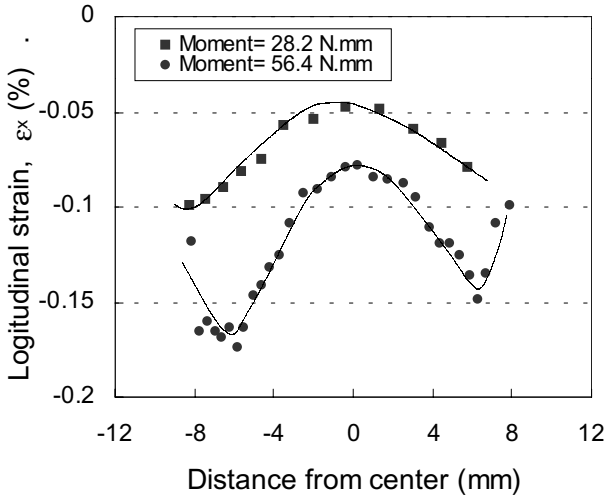

Fig. 8 Longitudinal strain distributions along the top of the molding compound in the four-point bending

While the bending moment was theoretically predicted to be uniform in the area between the two inner pins, the absolute value of the bending strain due to the moment was at a minimum in the center of the specimen and increased sharply in the vicinity of the chip boundary. It was ascribed to the much higher elastic modulus of the chip compared to the molding compound.

Average shear strains over each individual solder ball were determined by Eq. (2) with U and V fringe patterns, and plotted in Fig. 9. In mechanical bending, the strains were nearly zero in the center part containing 5 solder balls, and increased dramatically near the loading points. The maximum average shear strain, at the bending moment of 28.2 N.m, was 0.24%. At high bending moments, outlying solder balls tended to deform plastically as shown in Fig. 4(c).

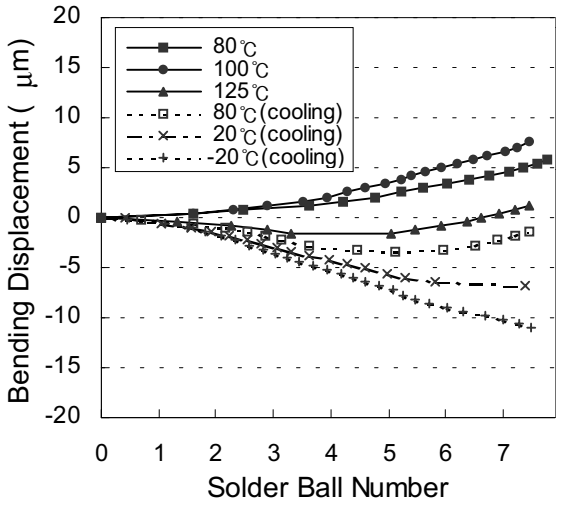

Fig. 10 Bending displacement distributions caused by temperature change

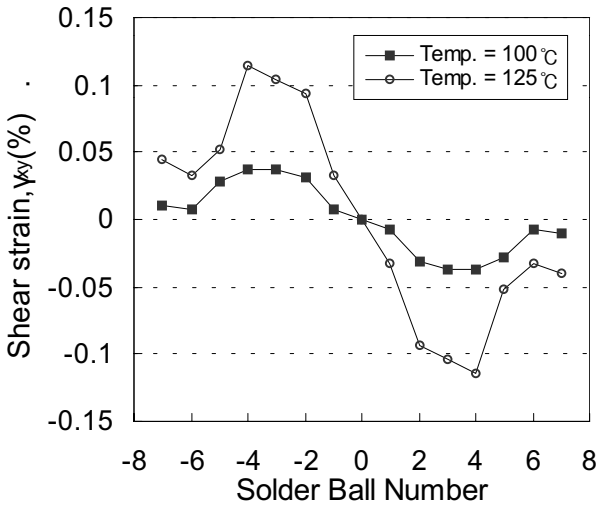

Fig. 12 Average shear strain distributions for WB-PBGA solder balls caused by temperature change

Thermo-mechanical Behavior

The bending displacements subjected to thermal load along the centerline of the package are plotted in Fig. 10. When the assembly was heated to 80°C, the PCB expanded more than the package because the equivalent CTE of the package is much lower than that of the PCB. This mismatch produced a global bending (∪) of the whole assembly as well as relative horizontal displacements between the top and bottom of the solder interconnections. The bending displacement increased as the temperature increased to 100°C. However, the bending displacement did not increase any further when the temperature increased further to 125°C. At a temperature higher than 100°C, the stress in the solder ball relaxes due to a creep deformation, and then the coupling between the package and the PCB is reduced. Instead, the coupling between the molding compound and the chip becomes dominant. Since the CTE of the molding compound is much higher than that of the chip, the opposite bending (∩) occurred in the part of the package including the chip. However, the sign (direction) of the bending curvature in the rest of the package remained unchanged. During cooling, the bending displacement increment was almost linearly related to the temperature increment relative to the configuration at 125°C.

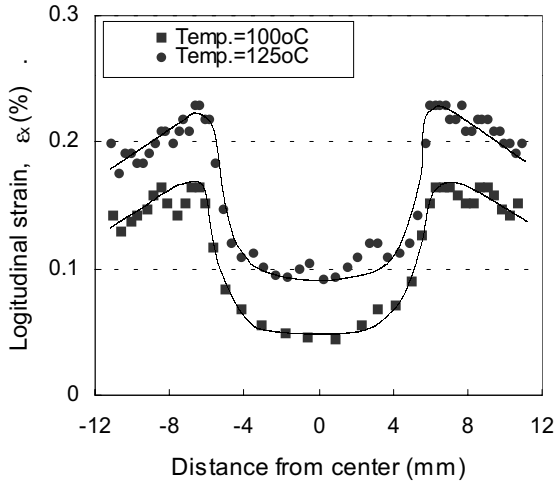

Fig. 11 Longitudinal strain distributions along the top of the molding compound caused by temperature change

Figure 11 shows longitudinal strain, ε_x distributions, along the top of the molding compound. The thermal load resulted in ensile strain on the top surface of the molding compound, whereas the mechanical bending produced compressive strain. This indicated that the thermal extension (tensile strain) was much more dominant than the bending strain (compressive strain) in the deformation of the package assembly subjected to thermal load. The dashed lines in the graph represent the boundary of the chip. Since the chip has a much lower CTE and a much higher modulus than the molding compound, the difference between strain values in the chip area and in the rest area was more severe than those in the mechanical bending .

Average shear strains over each individual solder ball were plotted in Fig. 12. In thermal loading, the solder ball located at the edge of the chip (no. 4 solder ball in Fig. 1) had the largest average shear strain, while that caused by the mechanical bending occurred in the end solder ball. This result is entirely different from the results for CBGA package assemblies, which have the largest shear strain in the rightmost or leftmost solder ball. The maximum average strain at 125°C was 0.12.

Comparison of Deformation Behavior

Figure 13 shows tip displacements (V displacements) corresponding to the bending moment and the temperature. They were calculated at the location between solder ball numbers 6 and 7 (x = 9.75 mm) with respect to the center point (x = 0 mm). In the case of the mechanical loading, the tip displacement increased linearly with the bending moment reaching about 8.8 μm at 42.3 N.m, and then increased more rapidly to the moment of 70.6 N.m. In the thermal loading, the tip displacement increased linearly with temperature increment, reaching about 5.7 μm at 100°C, and then decreased with temperature increment. The tip displacement at the temperature of 100°C was quite close to that at the moment of 28.2 N.m, which indicated that the package assembly bent by the moment of 0.176 N.m per 1°C in a linear elastic region

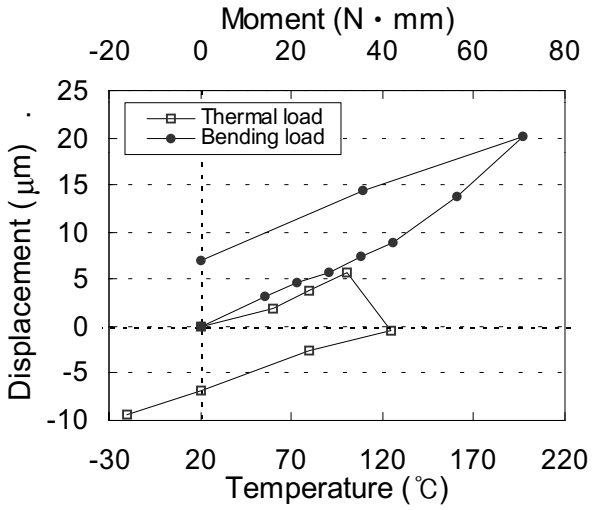

Fig. 13 Tip displacement according to the bending load and thermal load

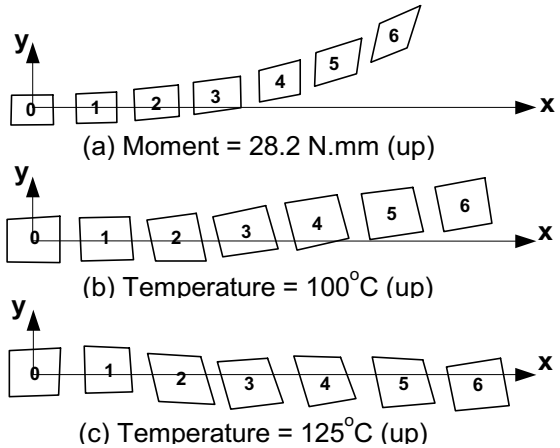

Fig. 14 Enlarged deformed shape of solder balls by the mechanical bending and the thermal loading

before the solder balls relaxed. In the unloading (cooling) processes in each case, the tip displacement decreased linearly with the decrement of moment (temperature) at the same rate as that of the loading (heating). As a result, the mechanical loading cycle produced permanent upward bending (∪), but the thermal cycle produced downward bending (∩).

As can be seen in Fig. 9 and Fig. 12, the sign (direction) of the average shear strain for thermal loading was opposite to that for mechanical bending. Figure 14 shows the deformed shapes of solder balls with displacements magnified by a scale factor of 200. For simplicity, the cross-section of the solder balls is represented as a rectangular shape consisting of the four corner points of the solder ball. It reveals that the solder balls experienced extension and shear strain as well as rigid body rotation. The shapes of solder balls deformed by thermal loading are clearly distinguishable from those caused by mechanical loading. The deformation mechanism of the package assembly by mechanical bending and thermal loading is illustrated schematically in Fig. 15. Suppose the solder balls have no stiffness so that the package and the PCB can deform freely. When the assembly is subjected to mechanical bending, the package and the PCB tend to bend individually, as shown in Fig. 15(a). When the two bodies are joined by solder interconnections, the assembly deforms together and the solder balls would experience positive shear strain. When the assembly is subjected to thermal loading, the PCB tends to expand more than the package, as shown in Fig. 12(b). When the two bodies are joined by solder interconnections, the solder balls would experience negative shear strain.

Conclusions

Thermo-mechanical and flexural behavior of a WB-PBGA package assembly was examined using high-sensitivity moiré interferometry. Detailed global and local deformations of the assembly by thermal and mechanical loading were

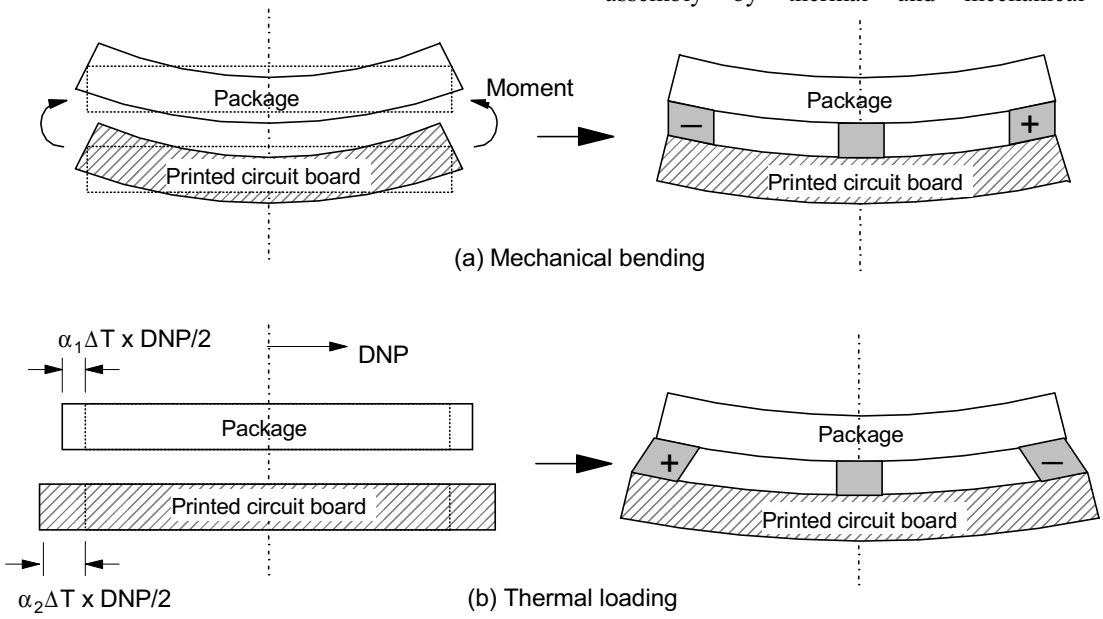

Fig. 15 Schematic illustrations of the deformation mechanism of the package assembly

investigated. The deformations caused by thermally induced bending were compared with those caused by mechanical bending.

The fringe patterns produced by temperature change were quite different from those produced by mechanical bending, while the apparent bending shapes were similar. The results revealed highly nonlinear behavior of the package assembly under thermal loading. Under thermal loading, the solder ball located at the edge of the chip has the largest average shear strain, while that caused by the bending moment occurs in the end solder. The sign (direction) of the shear strain caused by the mechanical bending was the opposite of that caused by the thermal load. The results also show that real-time moiré interferometry is a powerful and effective tool in experimental studies of electronic packaging.

Acknowledgements

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