

## *Session PR-2*

### *Packaging Reliability(2)*

#### *PR-2*

##### **Wafer Level Applied Near-Hermetic Protection for Semiconductors**

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##### **Evaluation of Thermal Shear Strains in Flip-Chip Package by Electronic Speckle Pattern Interferometry (ESPI)**

Woosoon JANG, Baik-Woo LEE, Dong-Won KIM, Dongil KWON, Seoul National University, Korea  
Jae-Woong NAH, Kyung-Wook PAIK, Korea Advanced Institute of Science and Technology, Korea

##### **Study on Microstructure and Shear Strength of the Sn-Ag-Sb Solder Joints**

Hwa-Teng LEE, Tain-Long LIAO, Ming-Hung CHEN, National Cheng Kung University, Taiwan

##### **Measurement of Thermo-mechanical Deformation of Wafer-Level CSP under Thermal Cycling Conditions**

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# Wafer Level Applied Near-Hermetic Protection for Semiconductors

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## Abstract

Military electronic parts are becoming unavailable. Weapon system designers are forced to use commercial plastic encapsulated microcircuits (PEMs). PEMs are susceptible to moisture related failure mechanisms occurring from long-term exposure to moisture even at very low humidity levels. Weapon systems must operate reliably after long-term dormant storage sometimes greater than 30 years. An Army Aviation and Missile Command Manufacturing Technology program is reviewed that provides a process for a potential near-hermetic wafer level seal for long term moisture exposure protection of PEMs. The process also provides potential benefits to the commercial semiconductor manufacturing community.

## Background

As the military and its suppliers struggle with COTS insertion issues, one particularly controversial area is whether standard commercial parts are sufficiently robust to operate under severe environments apparent in many military applications. This question has arisen as the military's share of the electronic component market has plummeted to less than one percent, making the defense industry's requirements insignificant compared to the consumer and telecommunications industries. Ceramic-packaged devices, long considered the gold standard for reliable packaging, are greatly diminishing as manufacturers steadily eliminate them from their product lines due to high manufacturing cost and low customer volumes. This lack of hermetic components has resulted in an availability gap that can only be filled by commercial parts.

Commercial Plastic Encapsulated Microcircuits (PEMs) are often manufactured using uniform, highly automated lines that produce very reliable parts for use in a typical office environment. But PEMs used in a harsh military environment may cause intermittent and catastrophic failures that are unacceptable in a battlefield situation. Missiles with shelf lives of 10-20 years and longer are expected to operate reliably after storage in harsh environments that PEMs are not designed to withstand. A good portion of failures are moisture related – water entering into the PEM and acting as a catalyst for corrosion on the integrated circuit (IC) die or interconnect bond pad. Epoxy materials used for encapsulation all absorb water to some degree, thus making top-layer IC metal protection a must. Silicon Nitride is most often used as a passivation layer on the surface of the die, but does not always provide a crack or pinhole-free conformal coating. Defects in

this passivation layer and around bond pad edges allow ionic contamination and moisture to enter; eventually destroying aluminum traces or contaminating interlayer dielectrics. Corrosion can also attack the wire bond interface (figure 1).

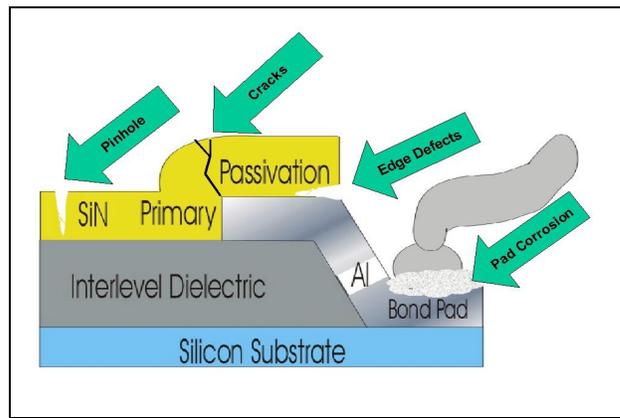
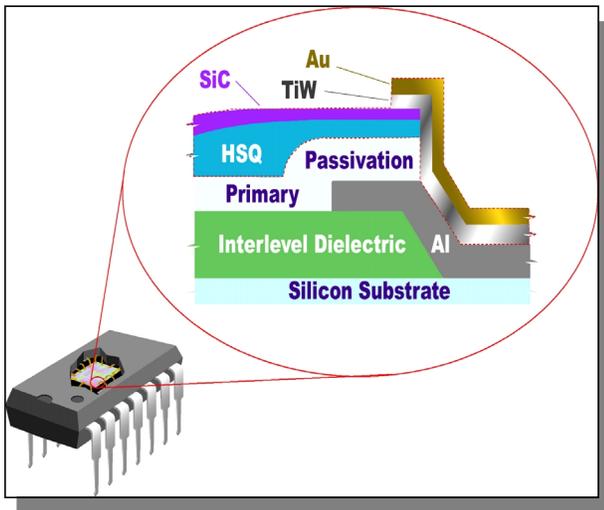


Figure 1 - Semiconductor Susceptibility to Moisture

The defense industry has tried various external IC protection methods including desiccants, external conformal coatings, specialized hermetic die packaging, and “cocooning” (a hermetic enclosure around the circuit card assembly). All except the latter two fail to provide adequate moisture protection. Specialized hermetic die packaging and cocooning, while effective, are expensive, and suffer from die availability problems and may be unsuitable for weight and volume-sensitive applications. Another alternative is chemical die removal from commercial plastic packages and repackaging them into hermetic modules; a possible small volume approach to solving obsolete component problems in legacy weapon systems. It remains to be seen if the repackaging process introduces latent failures that may appear later in a fielded system.

Since few viable reliability improvement solutions are available, weapon system integrators are forced to extensively test PEMs to see if they can withstand particular military environments. These qualification tests are very expensive and limit the selection of available parts. Unannounced material and process changes by the manufacturer can result in field failures and invalidate previous test results.

Military and non-military users all have to deal with PEMs assembly issues brought about by moisture sensitivity. The worst of these is “popcorning”, where entrapped moisture



**Figure 2 - ChipSeal® Near Hermetic Seal**

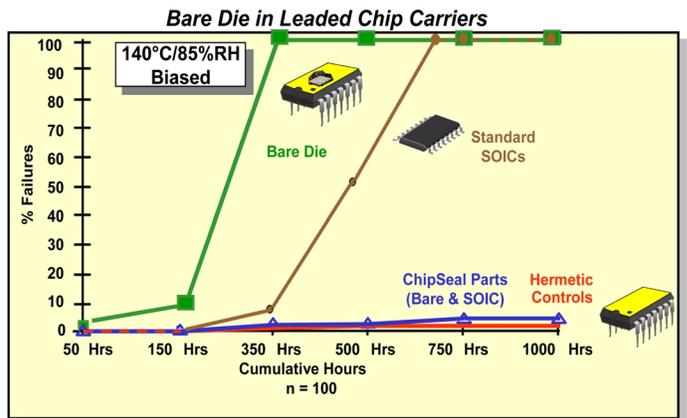
turns to steam during the solder reflow process and can only escape by forming a crack in the encapsulation, leading to immediate or eventual failure of the IC. In addition, advanced packaging such as flip chip and chip scale packages use little or no encapsulation to protect an IC from moisture, usually making advanced non-hermetic packaging unsuitable for military applications in harsh environments.

All these moisture-related reliability issues can make switching to COTS risky for military applications. To make PEMs a viable replacement for military-grade ceramic-packaged devices, the defense industry needs an inexpensive and effective scheme to demonstrate elimination of corrosion-caused failure mechanisms. This method must also add value to commercial applications in a way that encourages semiconductor manufacturers to adopt the protection method. The U.S. Army Manufacturing Technology (ManTech) Program has begun a project – “Wafer Applied Seal for PEM

Protection” (WASPP) to solve these problems by developing and demonstrating methods for applying protective coatings to semiconductor devices at the wafer level.

**Near Hermetic Coating**

Dow Corning’s ChipSeal® is a coating method that deposits layers of hydrogen silsesquioxane (trade name: Flowable Oxide – FOx®) and silicon carbide over the passivation on the surface of a semiconductor wafer. Two layers of metal are patterned over the silicon carbide and aluminum bond pads to provide a near-hermetic seal to each integrated circuit (figure 2). A recently completed Air Force program (contract F33615-93-C-1355) demonstrated ChipSeal® effectiveness with a survival rate approximating mil-spec hermetic parts during a 1000 hour Highly

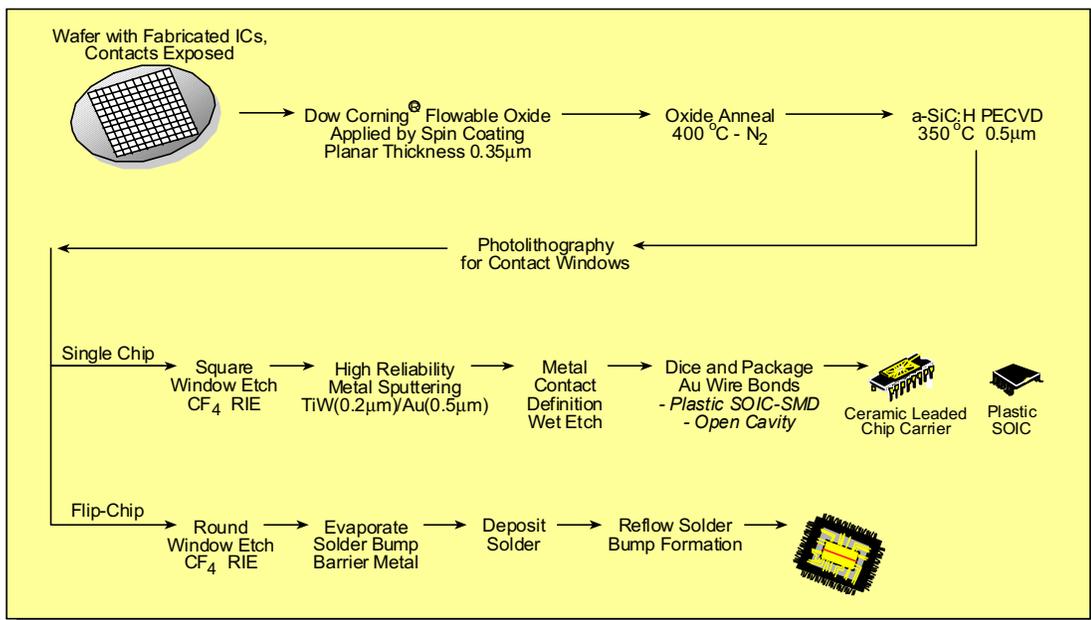


\*HAST exposure of plastic SOICs performed by ISE/IQL, San Jose, CA

**Figure 3 - ChipSeal® Coated vs Uncoated Reliability**

Accelerated Stress Test (HAST) (figure 3).

ChipSeal® is a chemically inert dielectric passivation that is non-corroding, compatible with all current interconnection approaches, and can be administered using standard process

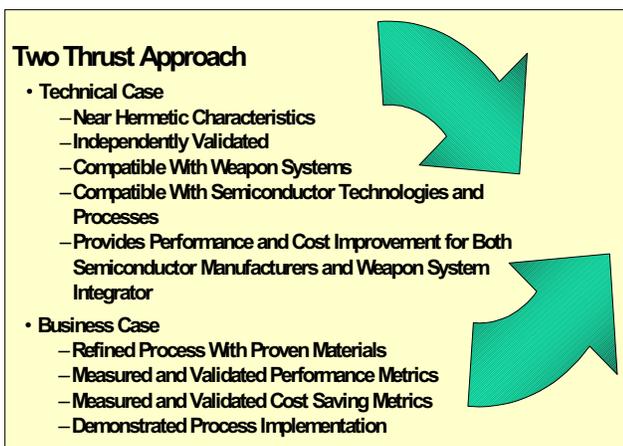


**Figure 4 – ChipSeal® Process Flow**

technology and equipment. Figure 4 shows the ChipSeal® process flow. The coating is an end of line process and can be applied either as an overcoat to the existing passivation or as a replacement for the primary passivation.

**Program Approach**

The WASPP Program takes a two-pronged approach to solving moisture-related PEMs problems by providing both technical and business solutions for weapon system integrators and the semiconductor industry. The technical approach is to develop a process that will provide near hermetic characteristics that can be independently validated with the process being compatible with both weapon systems and semiconductor technologies/processes. The business case will measure and validate performance and cost savings benefits for both the weapon system integrator and the semiconductor industry (figure 5).



**Figure 5 - WASPP Two Thrust Approach**

**Program Structure**

The WASPP Program is structured around a vertically integrated team that consists of the following:

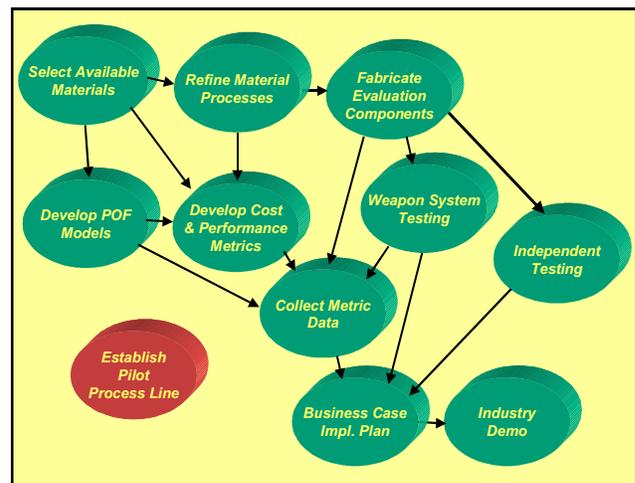
- End User - US Army Aviation And Missile Command
- Weapon System Integrator - Lockheed Martin Missiles And Fire Control
- Electronic Subsystem Integrator – Rockwell Collins
- Material Provider - Dow Corning
- Semiconductor Manufacturers - Fairchild Silicon Based Manufacturing) and TriQuint Semiconductor (Gallium Arsenide based Manufacturing)
- Packaging And Wafer Provider - Chip Supply
- Independent Test Organization - Amkor

Fairchild and TriQuint have expressed high interest in the potential for process cost reductions and performance improvements. All non-university team members, including

both semiconductor manufacturers, have invested their own funds in the project. Fairchild sees the enabling potential for advanced packaging at lower cost and TriQuint sees a potential to improve performance while maintaining low cost.

**Program Tasks**

WASPP project tasks are shown in figure 6. The project is not aimed at developing materials since materials are believed to be available that will meet military requirements. Rather, WASPP is aimed at selecting available materials and refining the material process to optimize the performance and minimize the cost of the materials. Plans are to produce actual parts with and without the coating process, collecting yield and other metrics during the fabrication. The parts will then undergo independent component tests and will also be qualification tested in actual weapon system electronic subsystems. Throughout the project, a cost benefits analysis will be performed with the development of a business case to assist widespread implementation by both the semiconductor industry and the weapons community. Another key part of WASPP is the development of a prototype production capability. The prototype facility will be built to permit early technology insertion, to assist semiconductor manufacturers in implementing the process, to provide a backup process for fabricators that have not yet implemented ChipSeal®, and as a tool to collect and demonstrate the business case metrics. The prototype facility will be capable of providing an overcoat to previously patterned wafers for encapsulation into plastic packages. The primary effort is to incorporate the process into the commercial manufacturing main stream but the prototype line will provide a stop gap interim solution. Preliminary analysis shows that although the prototype process will be more expensive than standard COTS parts, it



**Figure 6 - WASPP Program Project Tasks**

offers near hermetic benefits at lower cost than other existing solutions.

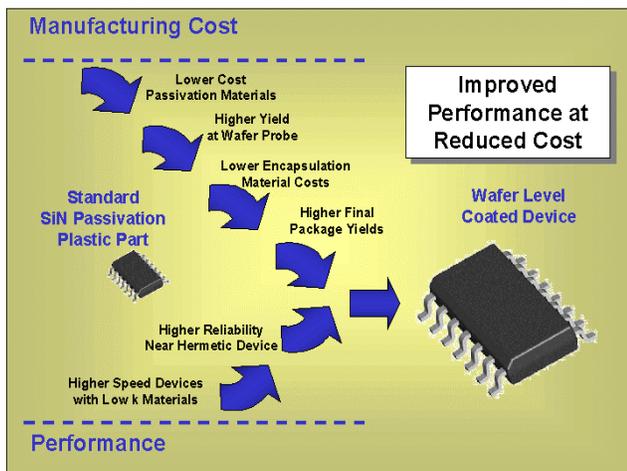
**Critical Goal**

A critical goal of this project is successful adoption of a near-hermetic protection process by as much of the semiconductor industry as possible. Wide adoption leads to more part choices and advanced technology benefits for the

military. For this to happen, semiconductor manufacturers must see economic and competitive value in using a coating that adds more steps and cost on top of an already complex manufacturing process. Initial analysis indicates several areas where value could be added by using the ChipSeal® process. Highly complex, multilayer integrated circuits can exploit low-k organic interlevel materials to improve on-chip circuit speeds and analog performance if the chip's surface is sealed to prevent the dielectric from absorbing water. Lower purity, cheaper packaging materials can be used since corrosion issues at the chip surface are no longer an issue. ChipSeal® adoption may also lead to greater flip chip, chip-on-board, and chip scale package acceptance due to corrosion elimination on bare die. Initial data shows a ChipSeal® coated device appears to better survive the rigors of wafer probing and packaging processes, leading to increased final packaged device yield. Other enhancements include improved safety from non-pyrophoric (non-igniting), non-toxic, non-corrosive precursor gasses. The Holy Grail in ChipSeal® adoption goes beyond just over coating the existing passivation on the wafer. If ChipSeal® is used as the sole IC passivation, it can potentially reduce implementation costs to less than the current passivation material of choice, silicon nitride. When this occurs, the semiconductor industry, system integrators, and the military will all enjoy the benefits of lower cost, higher reliability PEMs.

### Expected Benefits

What are the expected benefits? When fully implemented, the weapon system community will have access to a wafer coating process that provides higher reliability PEMs and permits a higher selection of components for use in military applications. The semiconductor industry will see the lower



**Figure 7 - Improved Parts at Lower Cost**

cost, higher performance parts due to lower cost packaging materials and potentially higher yields. The path to the lower cost and improved performance is depicted in figure 7.

### Rapid Test Techniques

Rockwell Collins has developed a technique for rapidly evaluating PEM devices for resistance to long-term dormant

storage failure mechanisms that is being included in this program. This technique also provides the potential for shortening semiconductor device reliability qualification test times. This process technique was included in the program for two reasons, first to shorten the time for evaluating the effectiveness of the coating processes being developed. Secondly, and more importantly, it provides the capability to offer a total solution for identifying parts with suitable long-term dormant storage resistance to failures for use in missile systems. The coating process under development only provides protection to moisture related problems and not for diurnal temperature cycle stresses. The rapid test techniques provide low cost effective methods of determining resistance of a PEM to both moisture and diurnal temperature stress failures. The rapid test method employs the following six test processes to determine the robustness of a PEM to survive long-term storage conditions:

- Impedance Spectroscopy
- Ion Extraction and Chromatography
- Glass Transition Measurement
- Component X-ray Examination
- Coefficient of Thermal Expansion
- Solder Lead Compliance

Impedance Spectroscopy measures in-line impedance changes across a frequency band that results from the development of corrosion when subjected to HAST conditions. Typically, corrosion forming on wire bond to bond pad and wire bond to lead frame is not detected until the corrosion has accumulated enough to completely open the circuit. This technique allows detection of the corrosion prior to the complete failure of the circuit.

The ion extraction and chromatography technique measures un-bound atoms contained in the specimen of plastic molding materials of the PEM. The molding material is pulverized with non-plastic materials removed. The resultant material is placed in water, heated under pressure and the water is extracted and measured for contaminants including chlorine, bromine, potassium, and sodium. The degree of contaminates indicates the susceptibility to moisture related failure mechanisms of the PEMs.

Glass transition temperature measurements ( $T_g$ ) are made using a differential scanning calorimeter to detect the  $T_g$ . X-rays of the components can discern different die, sizes, lead frame geometries, features and areas. Coefficient of expansion (CTE) measurements can also be made with made with thermal mechanical analyzers. All of these characteristics in-site into potential problems with diurnal temperature cycle stresses.

### Process Alternatives

The wafer level near hermetic seal process involves two major components, a robust hydrophobic passivation to protect the semiconductor silicon structure from moisture corrosion and contamination effects and a metalization layer to protect the passivation edges and the Aluminum bond pad interconnection from corrosion and purple plague effects. Both organic and inorganic materials were investigated as

candidates for the passivation layer protection and three different metalization schemes are in the process of being refined in the program.

**Passivation Material Selection**

The program objective is to develop new processes using existing materials that would provide near hermetic properties and not to develop new materials. With this in mind several classes of materials were researched as potential candidates consisting of both inorganic materials and organic materials. Potential cost, maturity, and performance issues were considered in the evaluation. The inorganic materials included the following:

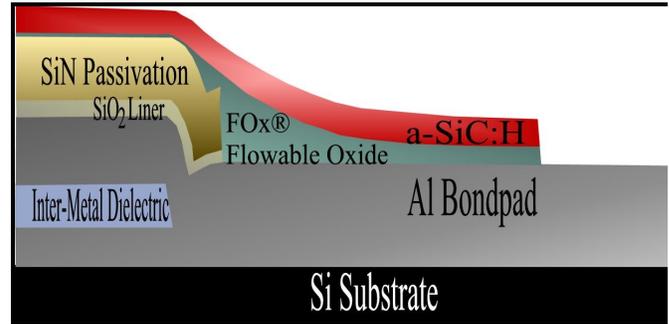
- Plasma enhanced chemical vapor deposition (PECVD) Nitrides
- Room-temperature, plasma deposition films
- Doped silicate glasses
- Silicon carbides

The organic material candidates included:

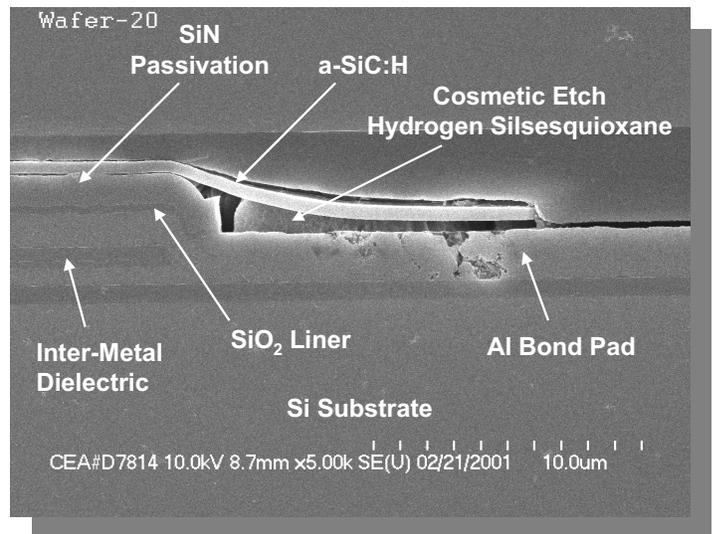
- Benzocyclobutanes
- Fluorocarbon polymers
- Polyimides
- Parylenes

The amorphous hydrogenated silicon carbide (a-SiC:H) films showed the most promise for both meeting the technical and cost objectives of the program, although some fluorocarbon polymers showed promise in meeting the technical requirements, they are not yet production ready but their development is being monitored. The silicon carbides had previously shown the capability to survive 1000 hours of biased HAST @ 130°C and 85% RH with less than 5% failures. The silicon carbides also exhibit lower dielectric constants with reduced water adsorption and use non-pyrophoric precursors offering improved safety. The incumbent silicon nitride passivations do not demonstrate near-hermetic properties. The a-SiC:H film properties are very similar to the incumbent SiN passivation materials with the notable positive differences shown in the table in figure 8. As it shows, the silicon carbide can be deposited faster, is safer, is more hydrophobic, and can be made to reduce stress

on the Si with a closer CTE. The silicon carbide process chosen uses the Dow Corning ChipSeal® coating scheme. This material is suitable to either replace the existing SiN passivation when implemented in the semiconductor manufacturing line or it can be applied to an existing wafer as a post overcoat process. Figure 9 shows a schematic representation of the overcoat process materials while figure 10 shows an actual scanning electron microscope picture of a cross section of an overcoated semiconductor. As the SEM indicates, the overcoat process produces a more planar



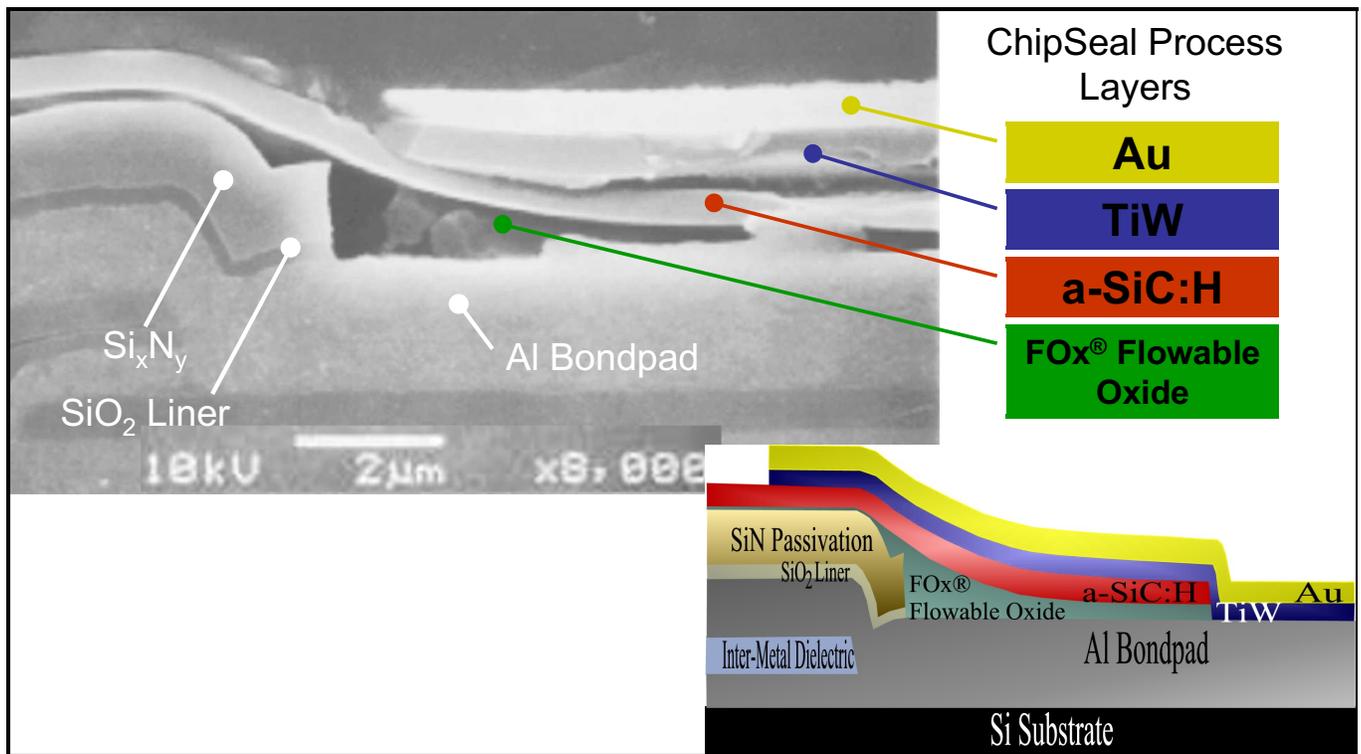
**Figure 9 - Overcoat Process Materials**



**Figure 10 - SEM of Overcoated Semiconductor**

Property	Silicon Nitride	Trimethylsilane based a-SiC:H
Deposition Rate (Å/min)	4500 — 8000	5000 — 10000
Pyrophoric	Yes	No
CTE (ppm/°C)	2.7	3 — 4
Intrinsic Stress (MPa)	+100 — -400	-50 — -200
Dielectric Constant	6 - 9	4 — 5.5
Moisture Induced Stress Hysteresis (%Δ @ 3000 hrs.)	≥ 4	≤ 0.8

**Figure 8 – Film Properties of a-SiC:H vs Silicon Nitride**



**Figure 11 - Baseline Metalization Protection (TiW/Au)**

topology with less stress areas than the standard silicon nitride passivation.

**Metalization Approaches**

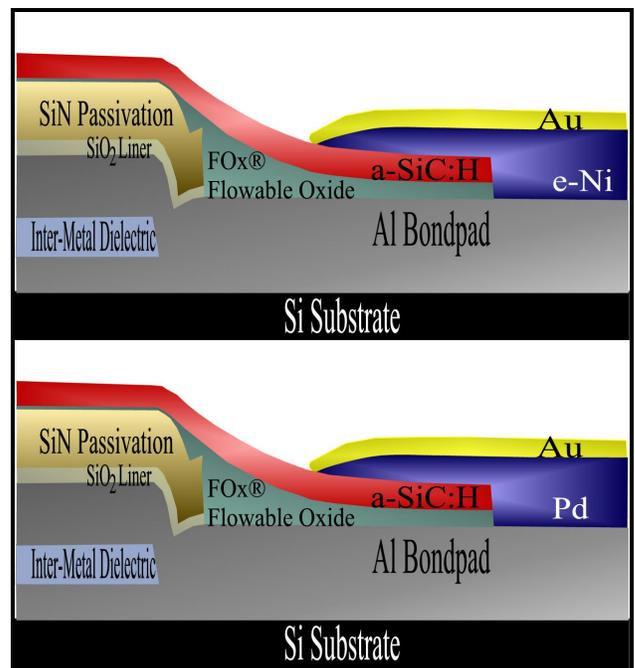
The baseline approach for the metalization protection consists of gold with a titanium tungsten barrier (TiW/Au) with gold being a noble metal providing protection from corrosion and the TiW providing a barrier for intermetallic migration of the gold into the aluminum bond pad. Figure 11 shows a schematic of the metalization overcoat along with a corresponding SEM of a TiW/Au overcoated semiconductor. The metals are both applied by sputtering in-situ. A 500 nm layer of Au provides the corrosion resistance while a 350 nm of TiW provides a barrier of the intermetallic formation. Photolithography and etching are required for field metal removal. Figure 12 shows an end of line direct replacement of the SiN passivation with the baseline silicon carbide

passivation sealed with the baseline TiW/Au metalization protection.

Two alternate metalization processes are also being investigated as potential lower cost methods than the TiW/Au method. The schematic of these two methods is shown in figure 13. The first of these alternatives is an electroless nickel and gold protection (e-Ni/Au). It is lower in cost than the TiW/Au



**Figure 12 - Baseline End of Line Passivation and Baseline TiW/Au Metalization**



**Figure 13 - Alternate Metalizations e-Ni/Au and Pd/Au**

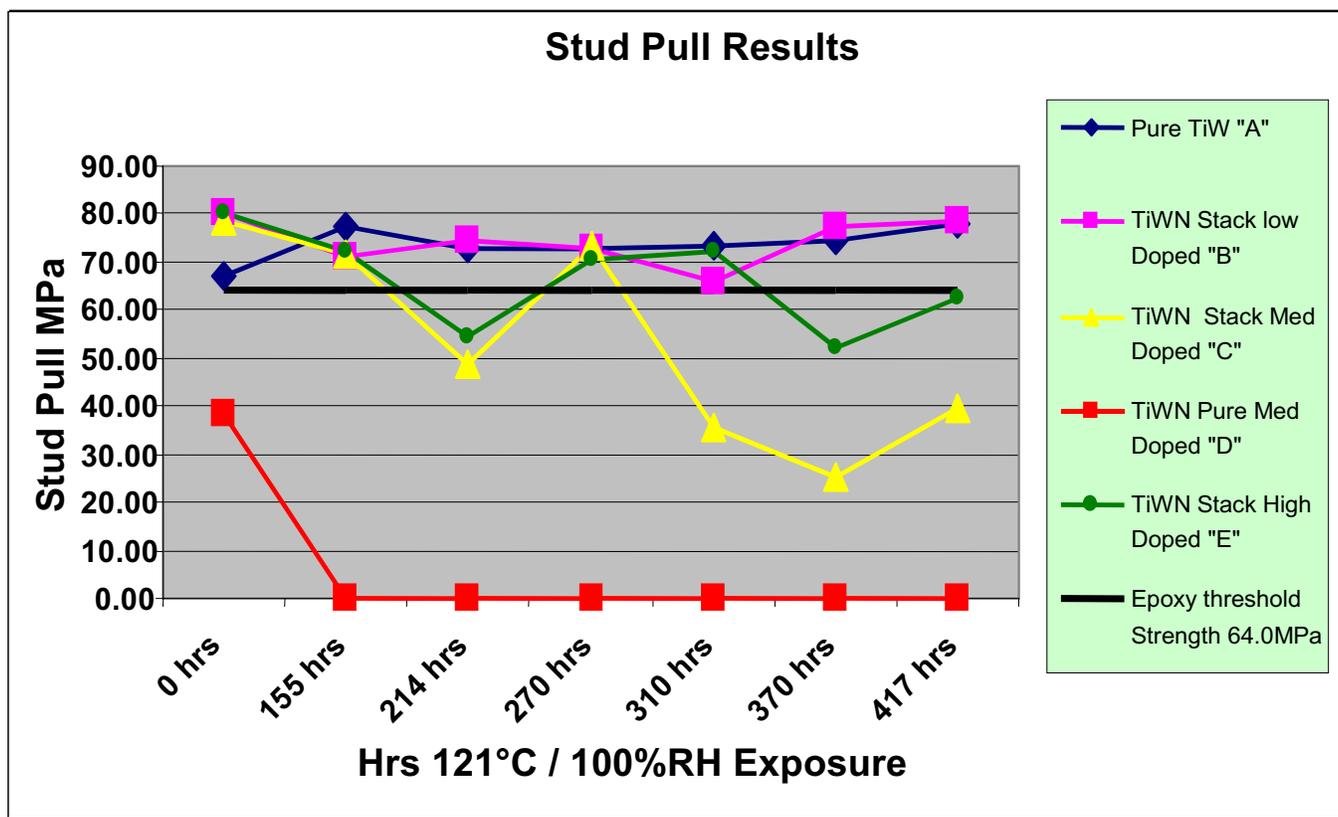


Figure 14 - N Doped TiW Pull Test Results

process because it eliminates extra masking steps. This process is also gaining acceptance as an under bump metalization (UBM) for advanced semiconductor packages. A Palladium gold (Pd/Au) protection scheme deposited as an ink that could be very low cost with high reliability is also being investigated. It offers a potential as a low temperature process and Pd has shown to provide a barrier to Au/Al inter-metallic formation. Further work is required to determine the strength of the Pd/Au stack to Al and to develop the costs of the process.

Other metalizations are also being evaluated with the passivation protection that may be because some technologies do not require the added metalization protection. Gallium Arsenide (GaAs) devices already use gold interconnections that are not susceptible to corrosion problems and therefore do not require the added metalization protection. Power semiconductor devices typically use larger aluminum wires attached directly to the aluminum bond pads. The mass of the aluminum in the power devices generally provides the needed corrosion resistance and adding a gold interface with the increased operating temperatures due to the high power only adds a potential for inter-metallic problems. In the case of power devices, an extra layer of aluminum sealing the passivation layer edges is being investigated as an alternative.

#### Latest Results

A post processing pilot line has been established and devices have been fabricated and tested with potential adhesion problems being uncovered. The basis for the poor adhesion was the nitrogen doping that was used in the TiW to

prevent the migration of the Au to the aluminum bond pad. Testing indicated pure TiW was a provided good adhesion with the AL and Au interfaces but it would not provide a very good inter-metallic barrier. A three layer approach to the TiW layer was tried with TiW/TiWN/TiW between the gold and aluminum and varying levels of doping were tried with pull tests and tests for inter-metallic formation tried on the different samples. This process was optimized with low levels of the nitrogen doping yielding the best results. The adhesion

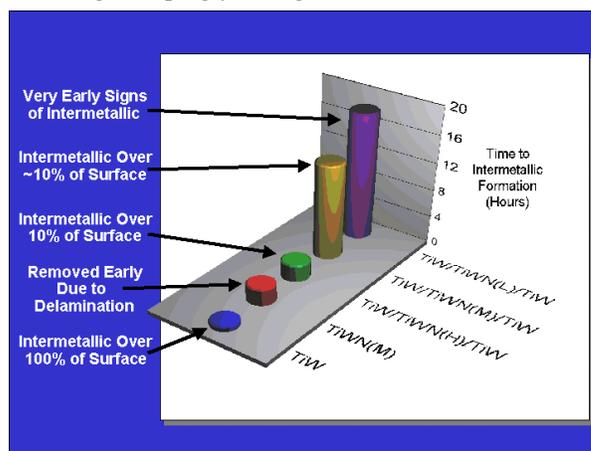


Figure 15 – Inter-metallic Formation Results

tests on the stack were performed using a standard stud pull test of the film stack. The results of the pull tests are shown in Figure 14. Inter-metallic formation time was measured to determine relative susceptibility to inter-metallic problems.

The results of the inter-metallic formation tests are shown in figure 15.

Sodium penetration tests were completed and shown the

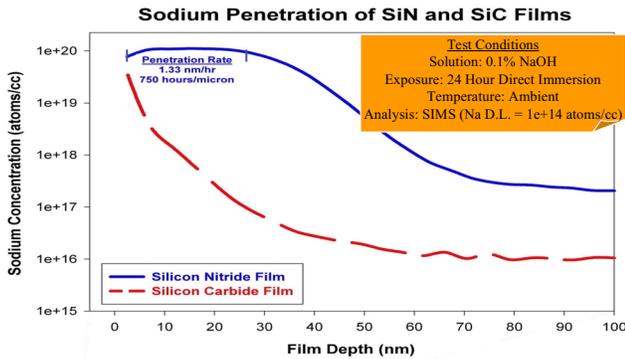


Figure 16 - Results of 24 Hour Exposure to NaOH

SiC passivation is much more resistant to the penetration of Na ions than the incumbent SiN passivation when exposed to sodium hydroxide. The results of the test are shown in figure 16.

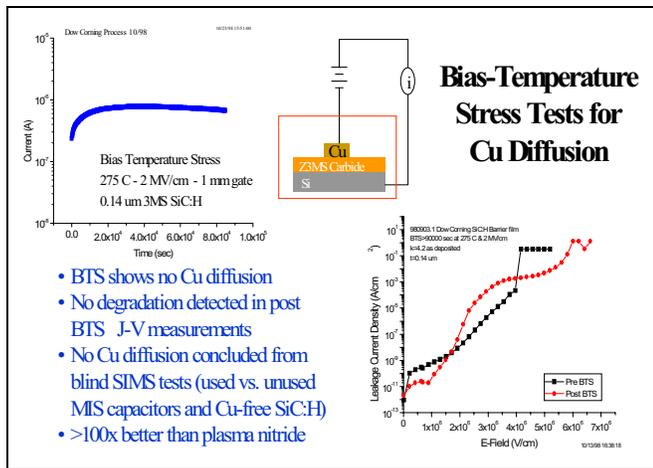


Figure 17 – Copper Diffusion Test Results

Copper diffusion tests were also performed on the SiC films and SiC was shown to be greater than 100 times as effective as nitrides in preventing the diffusion of copper. These results are shown in figure 17.

The first e-NI/Au devices have also been fabricated and the SEM of an e-Ni/Au device is shown in figure 18.

Galium Arsenide Devices have been fabricated as an in line process with outstanding results in terms of increased performance. The performance gained in the GaAs devices was achieved using low dielectric constant variations of the basic SiC at various levels in the device to achieve high performance device and still be able to maintain a near-hermetic seal at the passivation layer level. Speed performance gains of fifteen to twenty percent were achieved in the GaAs devices as shown in figure 19.

Several devices with the TiW/Au metalization scheme have been fabricated on the pilot line into complete functioning TSOIC packages and are being tested for robustness to failure mechanisms associated with long-term dormant storage. This sequence of testing includes unbiased HAST testing and temperature cycling. Yield information and cost metrics are also being collected from these fabricated parts. The parts will eventually be assembled into a military electronic subsystem and undergo full military qualification of the subsystem. The parts are also scheduled to undergo total dose radiation testing to insure nothing in the process will

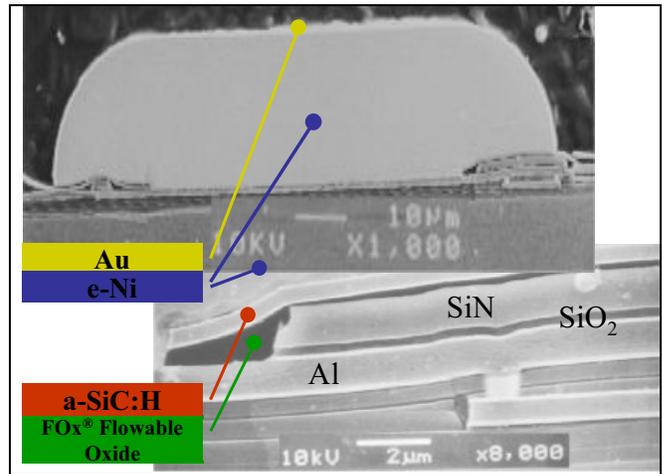


Figure 18 - SEM of e-Ni/Au Protected Device

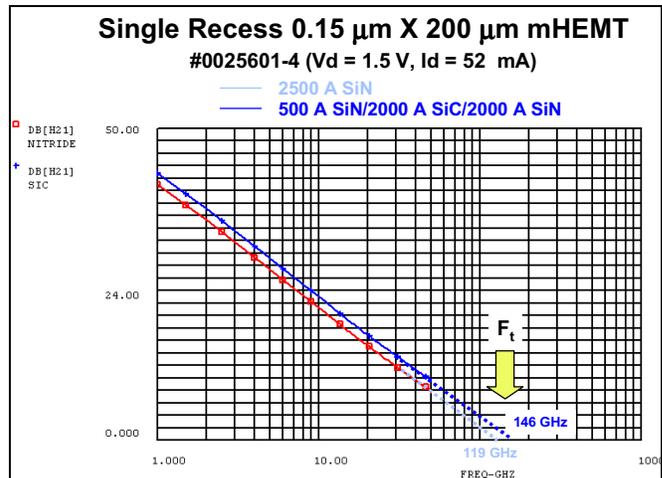


Figure 19 - Performance Improvement of GaAs Device

damage the inherent radiation tolerance of the device or its ability to be used in military systems. Since the testing is on going and this paper is being written prior to the oral presentation, additional results will be presented at the oral presentation.

### Workshops and Final Demonstration

The WASPP program has open semiannual government / industry workshops with a final demonstration will be held at the end of 2002 when the project ends.

### Conclusions

Although the program is still in the testing phase, evidence is being gathered that indicates, a robust near-hermetic seal applied at the wafer level can provide semiconductors with a low cost solution to provide semiconductors that can be used in harsh environments and can also provide required protection to the semiconductor package even in the minimally provided protection of the new emerging package technologies.

**Further Information**

The ManTech WASPP project is open to additional weapon system integrators and semiconductor manufacturers. For additional information, contact:

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# Study on Microstructure and Shear Strength of Sn-Ag-Sb Solder Joints

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## Abstract

This study investigates the microstructure, intermetallic compound (IMC) morphology and shear strength of Sn4.38Ag solder joints with different percentages of Sb content. The paper also evaluates, and compares, the thermal resistance of solder joints with different Sb content by means of high temperature storage testing.

In order to achieve solder joints of the size found in the BGA package, this study used pure copper wires of 1mm diameter as substrates for hot-dipping soldering. Solders with different compositions were selected for investigation, namely Sn4.38Ag, Sn3.9Ag0.9Sb, Sn4.4Ag1.44Sb and Sn4.11Ag1.86Sb, while a Sn40Pb solder was chosen for comparison purposes. High temperature storage testing was performed after soldering, with storage temperatures of 150°C and 200°C, respectively, and storage times of 0, 25, 100, 228 and 625 hours, respectively.

Experimental results show that most of the Sb which is added to the solder is soluted in the  $\beta$ -Sn matrix, with the remainder reacting with the Sn and Ag atoms to form an  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) compound. For temperature storage at 150°C for 625hrs, the addition of 0.9~1.44wt% Sb into the Sn4.38Ag solder is found to decrease the IMC thickness from 6.3 $\mu$ m to about 5.4 $\mu$ m. However, under the same storage conditions, adding 1.86wt% Sb increases the IMC thickness from 5.4 $\mu$ m to 7.1 $\mu$ m. Experimental results indicate that the shear strength of as-soldered solder joints increases with increasing Sb addition, i.e. the 1.86wt% Sb solder joint has a better as-soldered shear strength than either the 1.44wt% Sb or the 0.9wt% Sb joint. The shear strength values of these three joints are 119.5, 113.4, and 101.6 MPa, respectively, and it can be noted that all three values are higher than the shear strength of Sn4.38Ag, and of Sn40Pb, whose shear strengths are 78.4MPa, and 72.2MPa, respectively. After storage at 150°C for 625hrs, and at 200°C for the same period of time, the microstructures of the joints with 1.86wt% Sb content exhibit an  $\epsilon$  precipitation coarsening effect, which causes a reduction in its shear strength to a level which is lower than that of the 1.44wt% Sb joint. Therefore, the results show that the 1.44wt% Sb joint has the highest shear strength under high temperature and long-term storage conditions, i.e. the addition of 1.44wt% Sb into Sn4.38Ag solder yields the best thermal resistance.

## 1. Introduction

Due to environmental concerns, much effort has been directed at the creation, and development of lead-free solders within the electronics industry in recent years. Many lead-free alloy solder systems have been considered, with some such systems even being developed as far as the practical

packaging testing stage. Among the various feasible lead-free solder systems, the Sn-Ag solder system has attracted the most attention. Besides simply changing the proportion of Ag contained in the Sn-Ag solder, work has also focused on the inclusion of ternary, or quaternary elements, such as Cu, Bi, In, Sb and Zn. Addition of Sb into the Sn-Ag solder leads to several material property enhancements in the Sn-Ag-Sb joint due to its solid solution strengthening effect, including improved solder strength, better thermal resistance and a longer fatigue life. References relating to the Sn-Ag-Sb solder system include binary and ternary alloy phase diagrams [1-6], the mechanical properties of bulk solder [6-12], and the microstructure and interfacial reactions of solder joints [12-16].

The Sn-Ag-Sb ternary phase diagram [2-3, 5] shows the existence of  $\xi$ -Ag<sub>9</sub>(Sn,Sb), and  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) compounds, in addition to the SbSn compound, in the Sn-Ag-Sb system. Masson [2] also indicated the uniform distribution of the  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) compound from the Ag-Sn side to the Ag-Sb side in the Sn-Ag-Sb ternary phase diagram, thereby demonstrating the chemical stability of the  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) compound in an Sn-Ag-Sb system. Mason found that most of the Sb soluted in the  $\beta$ -Sn matrix in Sn-rich solders, and that the remainder participated in the formation of the  $\epsilon$  phase. However, in Sb-rich solders, most of the Sb reacted with Sn to form an SnSb compound, with the remainder again participating in the formation of an  $\epsilon$  phase [2, 5].

Adding 5% Sb to an Sn3.5Ag eutectic solder is found to increase its tensile strength from 35MPa to 55MPa, while the addition of 10% Sb increases this figure to 65MPa [11]. Reference [12] notes that the increase in tensile strength is accompanied by an increase in the hardness of the Sn3.5Ag joint. It is clear then that adding Sb improves the mechanical properties of an Sn3.5Ag solder. Previous studies, [12], indicated that the addition of 1.5% Sb yielded an improvement in both the adhesive strength, and the thermal resistance of Sn3.5Ag solder joints, although it also noted that the addition of Sb had the effect of raising the melting point of the Sn3.5Ag solder.

Compared to Sn3.5Ag solder, the properties of hypereutectic Sn4.38Ag and Sn4.38Ag solder joints with a small addition of Sb are still not well understood. Hence the aim of this study is to investigate, and evaluate, the effects of adding a small amount of Sb to such solders. The scope of the research includes the microstructure variation, the morphology of the interfacial intermetallic compound (IMC) layers, and the variation in shear strength. High temperature storage testing is performed to determine the microstructure evolution, the growth rate of the interfacial IMC layers, and the shear strength degradation of solder joints with different percentages



Fig. 1 As-soldered specimen.

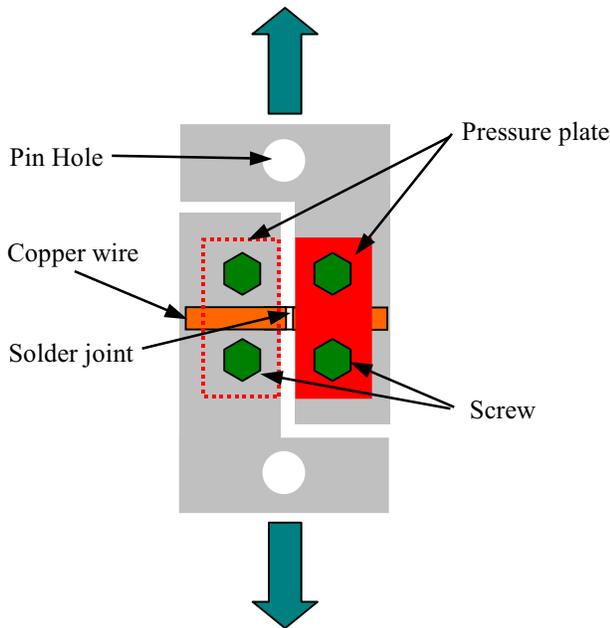


Fig. 2 Schematic representation of shear test.

of Sb addition.

Many testing methods have been developed to determine various mechanical properties of solder joints, including its tensile strength (adhesive strength), its shear strength, its isothermal fatigue life, and its thermomechanical fatigue life. Suitable methods for determining the shear strength of solder joints include the traditional pin and ring method [17], the solder ball shear test [18-20], the Iosipescu test [21-24], the single lap, or double lap method [25], the torsion method [26], and the asymmetrical four point bend method (AFPB) [27].

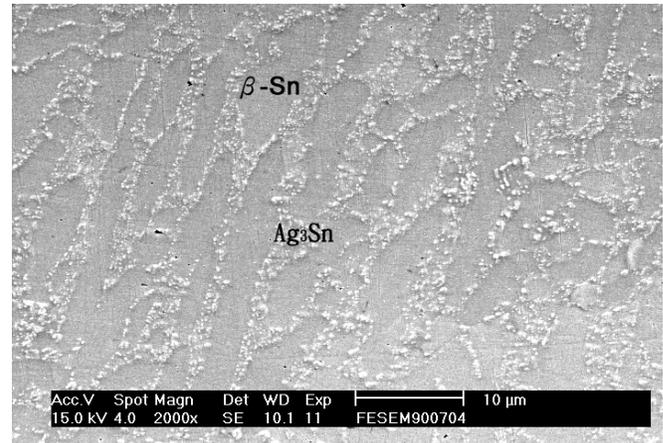
In order to achieve a representative size of solder balls, and due to fabrication concerns, this study involves copper wire of 1mm diameter. Lengths of this wire are soldered together, end by end, and the shear strength of various solder joints is then evaluated. [28].

## 2. Experimental Procedure

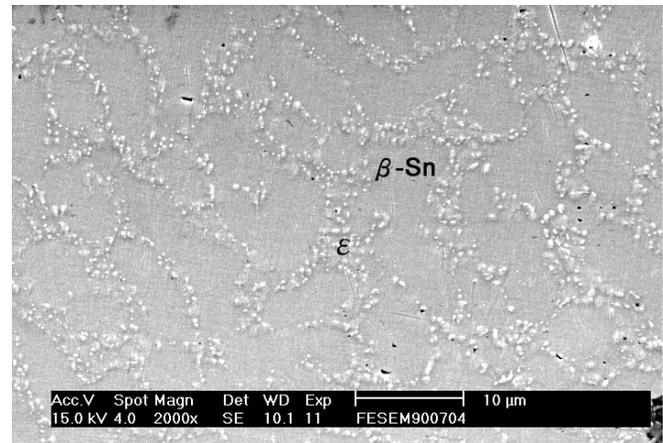
The copper wires used in this study were high-purity, electrolytic copper (99.9 wt%, in accordance with ASTM C11000). Solders were made by melting high purity Sn, Ag, and Sb in a crucible at 600°C. The actual compositions of the

Table 1 Composition of solders. (Unit: wt%)

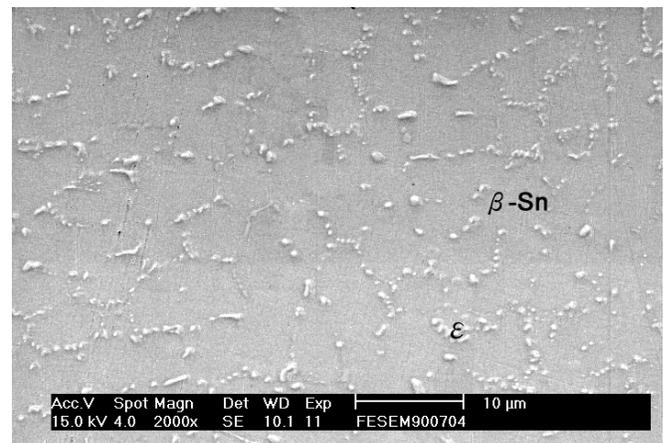
Solder/Composition	Sn	Ag	Sb
Sn4.38Ag	95.6	4.38	-
0.90% Sb addition	95.2	3.90	0.90
1.44% Sb addition	94.2	4.40	1.44
1.86% Sb addition	94.0	4.11	1.86



(a) Sn4.38Ag



(b) 0.9% Sb addition



(c) 1.86% Sb addition

Fig. 3 As-soldered microstructure of different soldered joints.

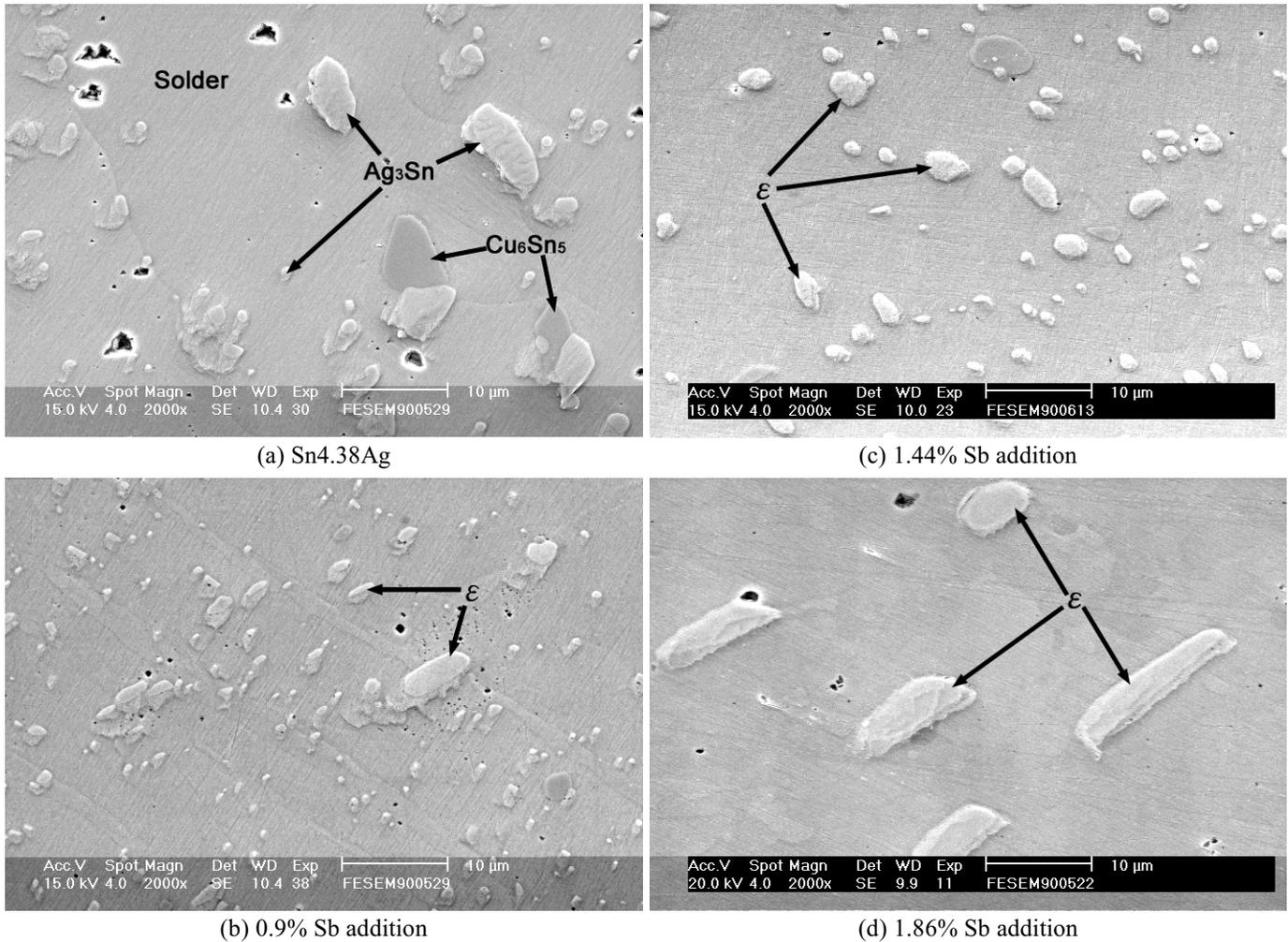


Fig. 4 Microstructures of Sn4.38Ag for different Sb Additions after 200°Cx625hours storage.

solder were examined, and identified by ICP-AES. The results are listed in Table 1.

The copper wires were first cut into 15mm lengths. The wire ends to be soldered were ground with SiC abrasive paper having a 1200 grit size, and were then fluxed with Taiyo electric BS-10 flux, produced in Japan. The copper wires were then clamped in a holder with a 0.3mm space between the two ends, and dipped in a solder bath set to about 300°C for 4 seconds. The wires were then allowed to cool in air. The resulting soldered copper wire is presented in Fig. 1. Next, the specimens were placed in an atmosphere furnace for high temperature storage tests, at 150°C and 200°C, respectively. An optical microscope (Leitz Metallux 3), and a Philips FEG XL-40 SEM were used to observe the resulting microstructure evolutions.

Shear strength testing was performed on a MTS 858 MiniBionix microtester, with the use of a double L- shaped holder, as shown in Fig. 2. The cross-head speed was set to 0.5mm/min.

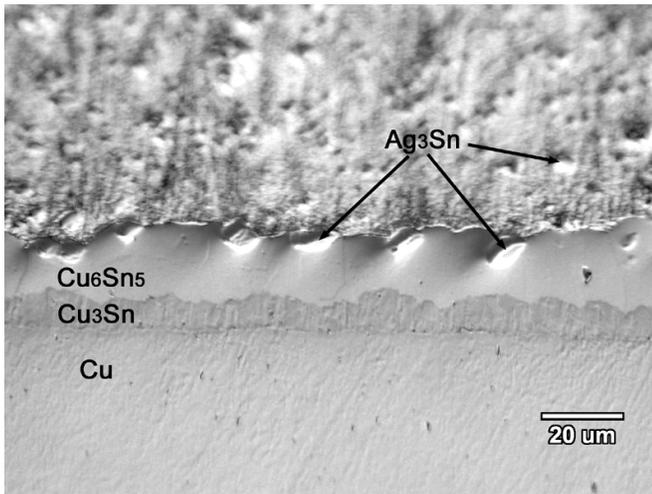
### 3. Microstructure Evolution

The as-soldered microstructure of Sn4.38Ag is shown in Fig. 3a, where the Ag<sub>3</sub>Sn compound is seen as white particles of 0.2~0.6μm, dispersed in ring-like forms throughout the β-

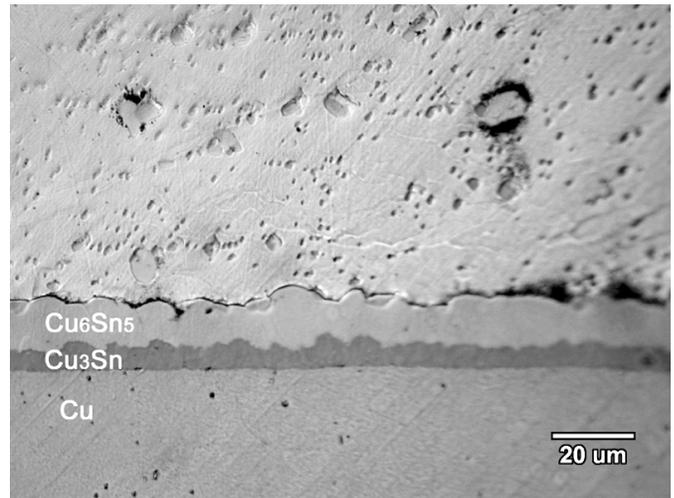
Sn matrix. Due to the hypereutectic composition of Sn4.38Ag, the Ag<sub>3</sub>Sn compound area is thicker than the one formed in eutectic Sn3.5Ag. Additionally, it may be observed that the microstructure features are long and narrow, and in fact, closely resemble a laminated structure. This is due to the rapid cooling rate, and explains why the average size of the microstructure width, i.e.3~4μm, is slightly different from that reported in previous literature (10μm diameter).

Fig.3b and Fig.3c show the as-soldered microstructure for the addition of 0.90%, and 1.86% Sb to the Sn4.38Ag solder material, respectively. The addition of Sb causes the original Ag<sub>3</sub>Sn compound in Sn4.38Ag to transform to ε-Ag<sub>3</sub>(Sn,Sb) [2-3, 5], and causes a gradual decomposition of the long and narrow microstructure of Sn4.38Ag as the percentage of Sb added increases. As may be seen in Fig.3b, the addition of 0.9% Sb causes the original long, narrow microstructure to become rounded, and the “ring” structure constructed by ε-Ag<sub>3</sub>(Sn,Sb) becomes thinner. With an addition of 1.86% Sb, the morphology of β-Sn is still rounded, but the ε-Ag<sub>3</sub>(Sn,Sb) compound has become semi-continually precipitated, and the particle size is much coarser than the original Sn4.38Ag.

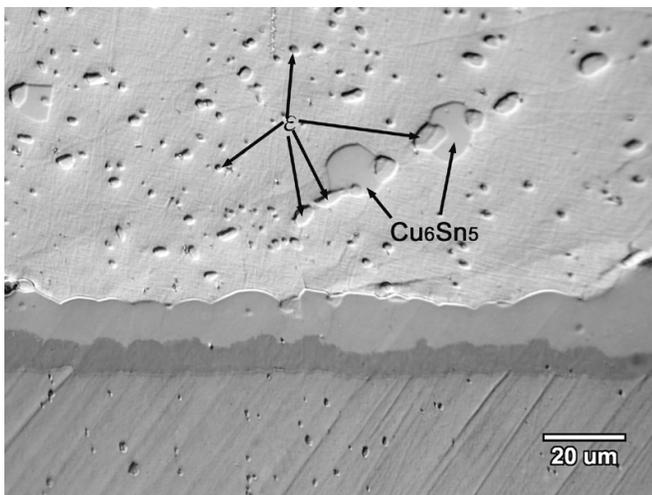
After storage at 200°C for 625 hours, Ag<sub>3</sub>Sn compounds of length 5~8μm, and coarse Cu<sub>6</sub>Sn<sub>5</sub> compounds are found in the



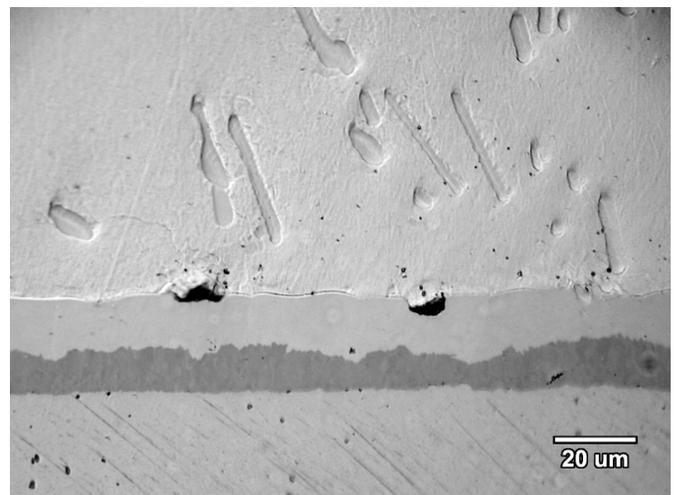
(a) Sn4.38Ag



(b) 0.9% Sb addition



(c) 1.44% Sb addition



(d) 1.86% Sb addition

Fig. 5 Interfacial IMC morphology variation of Sn4.38Ag for different Sb additions after 200°Cx625hours storage.

Sn4.38Ag, as shown in Fig. 4a. The existence of these compounds may be attributed to the excessive dipping temperature, which exceeded the eutectic temperature (231.9°C) of Sn-Cu systems, and which, therefore, caused the Cu to melt into the solder and to react with its Sn content. Adding 0.9% Sb (Fig. 4b) leads to an increase in the precipitation amount. Many fine particles are found in the matrix, and the number of large particles decreases proportionally. Apart from some large particles, the average particle size is around 1~2μm. As Sb addition increases to 1.44% Sb, (Fig. 4c), the fine particles disappear, to be replaced by a few, but large, particles of 2~5μm length. Due to the greater percentage of Sb added, the Ag<sub>3</sub>(Sn,Sb) particles are seen to be coarser than those which appear in Fig.4b, i.e. 0.9% Sb addition. With an addition of 1.86% Sb (Fig. 4d), the number of Ag<sub>3</sub>(Sn,Sb) particles is again reduced, but their size has continued to increase. The particles appear rod-like, and their size is 10μm. They are similar to, but larger than the Ag<sub>3</sub>Sn particles in Sn4.38Ag. It was also found that the presence of coarse particles reduced the effect of precipitation strengthening, thereby reducing the shear strength of the joint.

#### 4. Interfacial IMC Growth

As shown in Fig.5a, after soldering, two IMC layers are formed in the interface between the Sn4.38Ag solder and the wire's copper body, i.e. Cu<sub>3</sub>Sn and Cu<sub>6</sub>Sn<sub>5</sub>, identical to the case of Sn-Pb solders. Observation of the IMC layers using an optics microscope reveals that the interfacial structure remains unchanged as the percentage of Sb added increases, as shown in Fig. 5b ~ Fig. 5d. However, Vianco [15] and Blalock [4] found evidence of a micro-migration of Sb in the interfacial IMC layers, and the binary phase diagram [1, 4] showed that Sb could react with both Sn and Cu to form IMC layers. Therefore, from the point of view of qualitative analysis, it would appear that the mechanism of interfacial IMC layers of Sn-Ag-Sb solders soldered with Cu is still not well understood. However, based upon OM and SEM observations, the growth mechanism of interfacial IMC layers still appears to be via diffusion [12].

The factors which influence the growth of the interfacial IMC layer include the solder elements, the relative composition of these elements, soldering temperature, soldering time, storage temperature, and storage time. The

precipitated particles are a further, important factor. As shown in Fig. 5a, where the interfacial IMC layers in Sn4.38Ag contact the  $Ag_3Sn$  particles in the solder, they stop growing because neither the Sn, nor the Cu atoms are able to diffuse through the  $Ag_3Sn$  particles. In other words, the interfacial IMC layers have to grow around the  $Ag_3Sn$  particles. As mentioned above, many fine particles are precipitated after the addition of 0.9% Sb. Fig. 5a and Fig. 5b illustrate the obstruction effect on interfacial IMC growth of these precipitated particles. As Sb addition increases to 1.44%, the  $Ag_3Sn$  particles continue to suppress the growth of the interfacial IMC, and the IMC thickness is seen still to be thinner than Sn4.38Ag. However, with an addition of 1.86% Sb, the obstruction effect is substantially reduced due to the excessive coarseness of the precipitated particles, and therefore it may be seen that the IMC thickness in Fig. 5d (1.86% Sb) is thicker than in Fig. 5a (Sn4.38Ag). The influence of Sb addition on interfacial IMC thickness is shown in Fig. 6. When heating storage is carried out at 200°C for 625 hours, adding 0.9% Sb to the Sn4.38Ag decreases the IMC thickness from 23.5 μm to 18.1 μm. However, an addition of 1.86% Sb results in an increase of the IMC thickness to 25.0 μm. It is therefore obvious that the interfacial IMC thickness may be effectively suppressed if the precipitated  $Ag_3Sn$  particles are fine, and numerous. Furthermore, it is found that the IMC / solder interface is flattened under these same particle precipitation conditions.

### 5. Shear Strength Variation

The maximum shear strength was shown experimentally to occur at a displacement of about 0.1 mm, as shown in Fig. 7. As the displacement is increased further, the Cu / solder interface begins to crack, causing a rapid reduction in the shear strength of the joint. Crack propagation along the Cu / solder interface continues until failure of the specimen.

Fig. 8 shows the variation of shear strength over storage time of Sn4.38Ag solder joints with different percentages of Sb addition, when stored at 150°C. The as-soldered shear strength of Sn4.38Ag is 78.4 MPa. After 25 hours of storage,

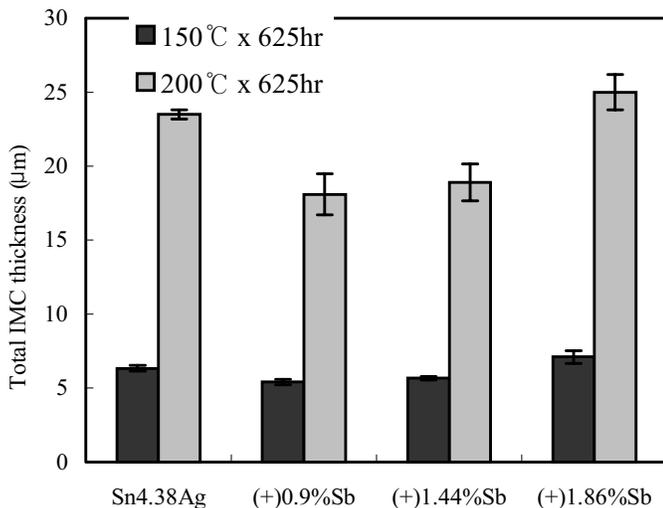


Fig. 6 Influence of Sb addition on interfacial IMC growth for Sn4.38Ag solder joints.

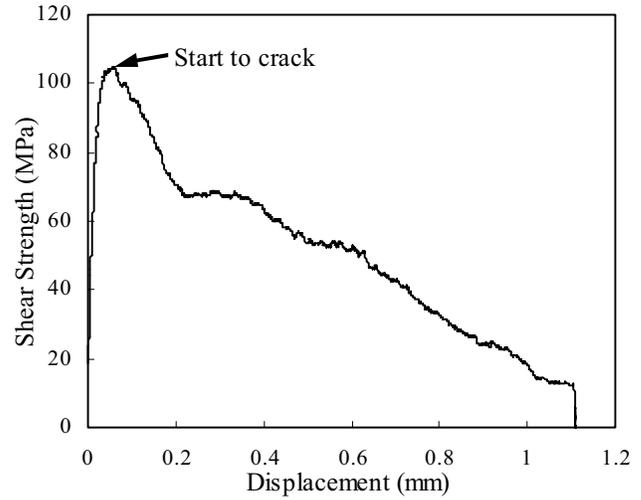


Fig. 7 A representative shear strength-displacement diagram (Sn3.9Ag0.9Sb, as-soldered).

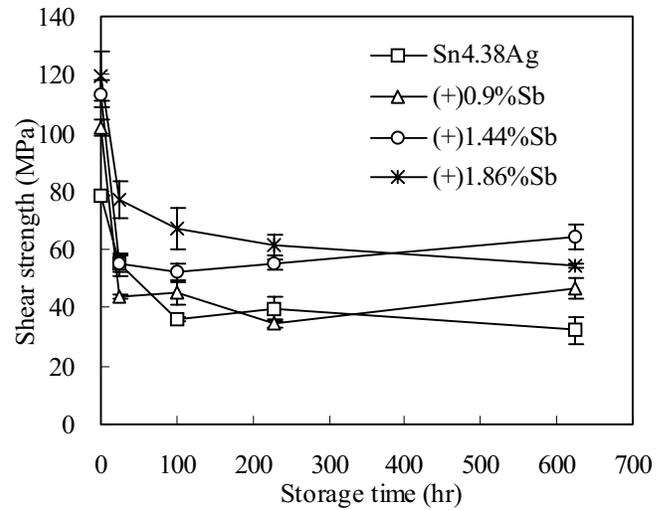


Fig. 8 Shear strength variation of Sn4.38Ag solder joints with different Sb addition under 150°C storage.

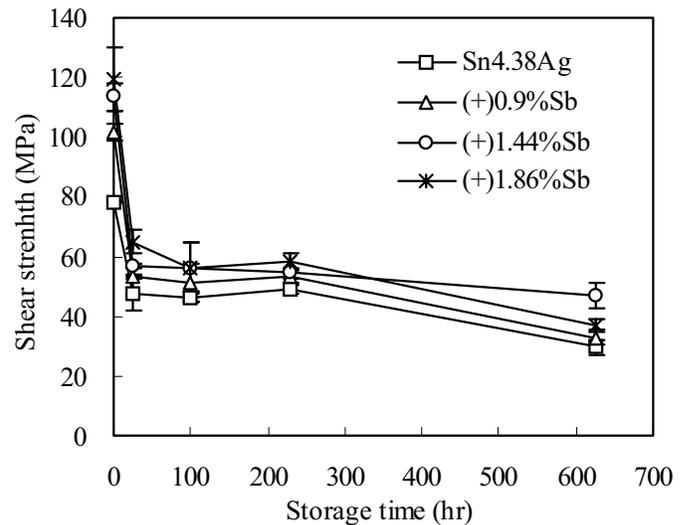


Fig. 9 Shear strength variation of Sn4.38Ag solder joints with different Sb addition under 200°C storage.

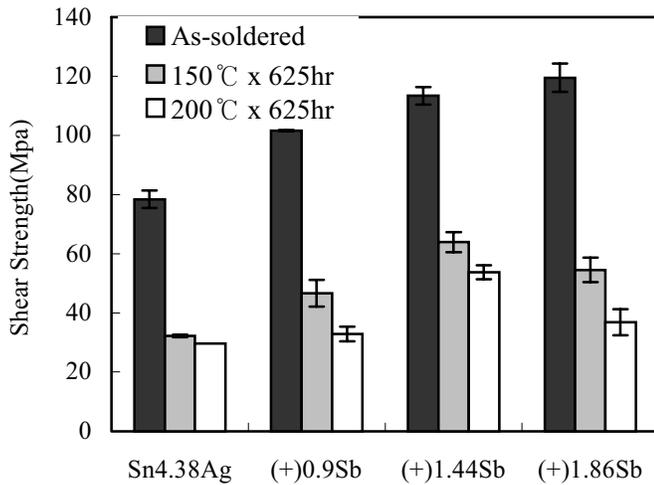


Fig. 10 Shear strength comparison of Sn4.38Ag solder joints with different Sb addition.

the shear strength decreases substantially to 55.2MPa, due to the tempering effect which occurs in high temperature storage. Under these storage conditions, the solder hardness decreases rapidly after a short storage time, leading indirectly to a weakening of the solder joints. The as-soldered shear strengths for 0.9%, 1.44%, and 1.86% Sb addition are 101.6, 113.4, and 119.5MPa, respectively, all of which are higher than Sn4.38Ag. It is clear then that the as-soldered shear strength increases with increasing Sb addition. This may be attributed to the solid solution strengthening of Sb in the  $\beta$ -Sn matrix, which enhances the strength of the bulk solder. Therefore the shear strength of the solder joints increases with increasing Sb addition because the difference in the relative strength of the solder and the Cu decreases [28].

After high temperature storage, the shear strength of the solder joints with Sb addition decreases substantially, although their strengths still remain higher than that of Sn4.38Ag subjected to the same storage conditions. The shear strengths of the solders with 0.9% and 1.44% Sb addition both show a “bounce effect” after 228 hours of storage; demonstrating an increment of approximately 10MPa. It is conceivable that this effect might be caused by the micro-migration of Sb in the interfacial IMC layers [4, 15]. After 625 hours of storage, the shear strength of the solder with 1.86% Sb addition is lower than that of the solder with 1.44% Sb. As mentioned previously, adding 1.86% Sb causes the  $Ag_3(Sn,Sb)$  particles to increase in length to about  $10\mu m$ , and reduces the number of precipitated particles, thereby softening the solder and, therefore, the solder joints. The bounce effect is counteracted by this excessive softness, causing the shear strength of the 1.86% Sb solder to be lower than the specimens.

Fig. 9 shows the variation of shear strength over storage time of Sn4.38Ag solder joints with different percentages of Sb addition, when stored at  $200^\circ C$ . As in the case of storage at  $150^\circ C$ , the shear strength of both the Sn4.38Ag, and the solders with Sb addition, decrease substantially after high temperature storage. As before, the figure demonstrates that Sb addition leads to an increase in material strength. However,

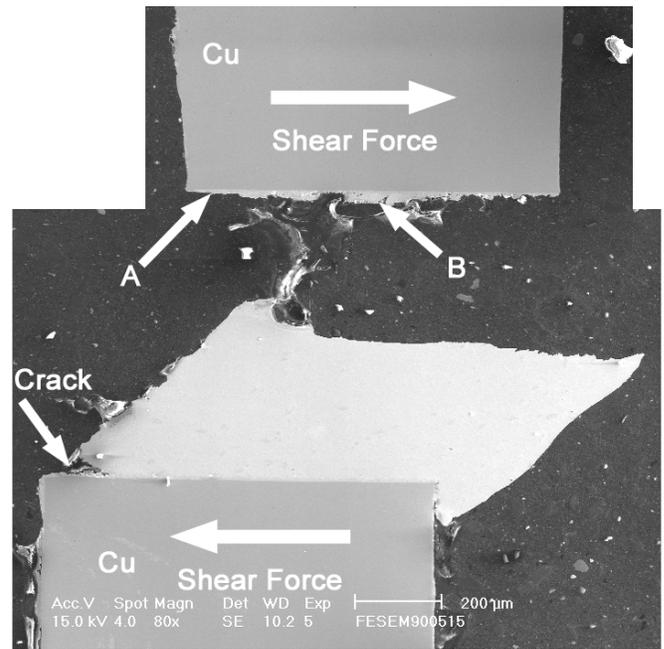


Fig. 11 Cross-section of tested Sn4.38Ag solder joint with 0.9% Sb addition, stored at  $200^\circ C$  for 625 hours.

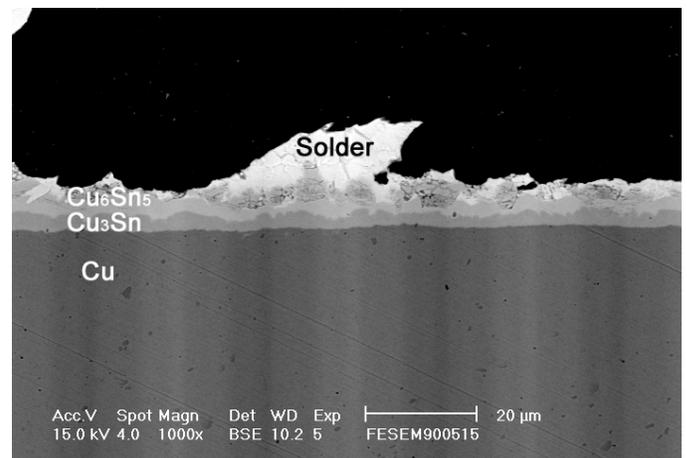


Fig. 12 Detailed view at point A in Fig. 11.

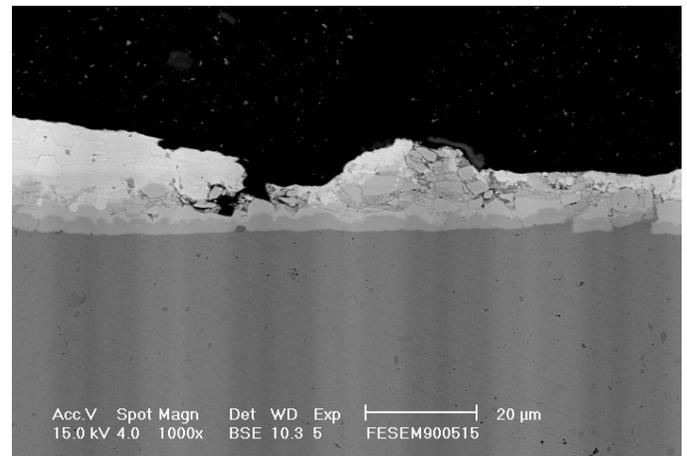


Fig. 13 Detailed view at point B in Fig. 11.

the bounce effect evident in the previous case is not present under this set of storage conditions. The absence of this effect may be due to the high temperature of 200°C (equal to 0.94T<sub>m</sub> for Sn4.38Ag), since the elevated temperature accelerates the diffusion rate of the Sb atoms, and substantially decreases the duration of the micro-migration phase.

Finally, Fig. 10 provides a comprehensive summary of the shear strength variation results. In the as-soldered condition, shear strength is seen to increase with increasing Sb addition, with a 1.86% Sb addition yielding the highest shear strength (119.5MPa). However, for both heating temperature / storage combinations, the shear strength peaks with an addition of 1.44% Sb. Hence the best compromise between shear strength and thermal resistance is obtained by adding 1.44% Sb to Sn4.38Ag.

## 6. Fractographic Analysis

The cross-section of the tested specimens was observed under SEM. The results show that fracture occurred along the solder/IMC interface, as shown in Fig. 11. In all cases, the initial damage was located at one of the two soldering interfaces facing the displacement direction (i.e. the position of maximum stress concentration) due to the discontinuity of materials. Correlating to the results in Fig. 7, no cracking occurred prior to reaching the maximum shear strength, and in this phase, the shear strength increased rapidly with increasing displacement. At the point of maximum shear strength, a crack occurred at the soldering interface, resulting in a substantial decrease in shear strength as displacement continued to increase. The crack propagated along the soldering interface until the specimen failed.

Fig.12 presents a high magnitude SEM observation, which shows that the position of the initial damage is more accurately located at the solder / IMC interface. The propagation of the crack is slightly deflected to the solder, as shown in Fig. 13.

## Conclusions

1. In the as-soldered condition, the long and narrow microstructure of Sn4.38Ag decomposes gradually as Sb is added. With an addition of 0.9% Sb, the original microstructure becomes rounded and the “ring” structure constructed by the  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) becomes thinner. With an addition of 1.86% Sb, the morphology of  $\beta$ -Sn is still rounded, but the  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) compound becomes semi-continually precipitated, and coarsens.
2. After 625 hours of storage at 200°C, rod-like particles of Ag<sub>3</sub>Sn of length 5~8 $\mu$ m are precipitated in the  $\beta$ -Sn matrix for Sn4.38Ag. However, the addition of 0.9% Sb, causes precipitation of numerous fine  $\epsilon$ -Ag<sub>3</sub>(Sn,Sb) particles of length 1~2 $\mu$ m, and the number of large particles decreases proportionally. As the percentage of Sb addition is increased to 1.44%, the precipitation of fine particles decreases, to be replaced by larger particles with length 2~5 $\mu$ m. With an addition of 1.86%, the number of particles precipitated decreases, and the particles once again become rod-like, and have a length of 10 $\mu$ m, i.e. they are larger than the original Ag<sub>3</sub>Sn particles in Sn4.38Ag. The excessive coarseness of the Ag<sub>3</sub>(Sn,Sb)

particles leads to a softening of the solder, and a subsequent decrease in its shear strength.

3. Adding 0.9% Sb into Sn4.38Ag results in the precipitation of numerous fine Ag<sub>3</sub>(Sn,Sb) particles, which directly obstruct the growth of interfacial IMC layers. Hence the IMC thickness for 0.9% Sb addition is thinner than in the case of Sn4.38Ag. As Sb addition is increased to 1.44%, the IMC thickness still remains thinner than for Sn4.38Ag, but at an addition of 1.86% Sb, the IMC thickness exceeds that of Sn4.38Ag due to a decrease in the number of Ag<sub>3</sub>(Sn,Sb) particles precipitated, and their coarseness, both of which factors reduce their ability to obstruct IMC layer growth. Under storage at 200°C for 625hours, adding 0.9% Sb to Sn4.38Ag leads to a decrease in the IMC thickness from 23.5 $\mu$ m to 18.1 $\mu$ m, while adding 1.86% Sb increases the IMC thickness to 25.0 $\mu$ m. Hence it is seen that numerous, fine Ag<sub>3</sub>(Sn,Sb) particles suppress the growth of interfacial IMC layers.
4. Regarding the as-soldered condition, the shear strength values of Sn4.38Ag, and solders with 0.9%, 1.44% and 1.86% Sb addition, are found to be 78.4, 101.6, 113.4, and 119.5MPa, respectively. In other words, the as-soldered shear strength increases with increasing Sb addition. However, after storage at 150°C for 625 hours, and at 200°C for 625 hours, it is found that maximum shear strength occurs for an addition of 1.44% Sb. Therefore the best compromise between shear strength and thermal resistance is obtained by adding 1.44% Sb to Sn4.38Ag.
5. Under heat storage at 150°C, a bounce effect occurs after 228 hours of storage in the case of the soldered joints with 0.9% Sb, and 1.44% Sb addition, which gives a shear strength increase in the order of 10MPa.
6. The shear test reveals that fracture of the joint occurs along the soldering interface. A high magnitude SEM observation of the specimen reveals that the precise position of the initial damage occurs at the solder/IMC interface.

## Acknowledgments

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# Evaluation of Thermal Shear Strains in Flip-chip Package by Electronic Speckle Pattern Interferometry (ESPI)

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## Abstract

In this study, we measured the thermal deformations of flip-chip solder joints by an electronic speckle pattern interferometry (ESPI) system. For the scale of evaluation required, the measured displacement resolution was modified to allow application to micro materials with long working-distance microscopes, iris and zoom lens. The flip-chip, a micro material constructed with silicon chip, printed circuit board (PCB) and Sn-36Pb-2Ag solder, is shear-deformed by temperature changes from 25°C to 125°C in a thermal vacuum chamber. From our experimental results we were able to deduce that the thermal expansion difference between the chip and PCB leads to shear strain at the solder joint. The local deformations of solder balls were measured at a sub micrometer scale, and the local shear strains of the solder balls were calculated from the measured displacements. In addition, the experimental results from ESPI demonstrated that the thermal deformations are similar to those results predicted from finite element analysis (FEA).

## Introduction

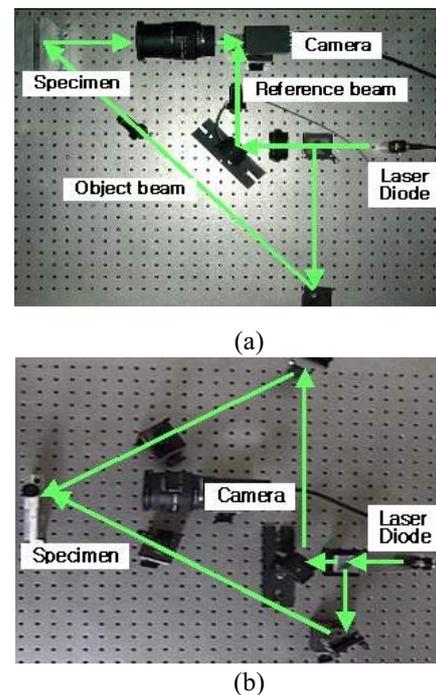
Although interest in micro fabrication techniques has been rising over the past several years, the development of evaluation techniques for these micro devices has not matched that of their fabrication technologies. So further development of micro deformation measurement techniques is required for evaluating the reliability of micro materials. In particular, non-destructive evaluation methods are of great interest to the industrial field because of the capability for real-time measurement during operation.[1]

Electronic speckle pattern interferometry (ESPI), one of the non-destructive evaluation techniques for investigating micro reliability, measures the micro deformation by laser speckle interferometry. Fig. 1 shows the principle of the ESPI system. Both out-of-plane (Fig. 1(a)) and in-plane (Fig. 1(b)) deformation can be measured. The laser source beam is divided into an object and a reference beam, and the interference between these two beams results in speckle pattern. As the object moves, the speckle pattern changes. By subtracting the deformed speckle pattern from the undeformed one, correlation fringes are produced which represent the deformation of the object. This fringe is analyzed by an image-processing computer, and converted into a quantitative value.

Fig. 2(a) and (b) display the principles of out-of-plane and in-plane deformation measurement. From the geometrical relationship, the displacement  $d$  is given by

$$d = \frac{f\lambda}{\sin \alpha + \sin \beta} \quad (1)$$

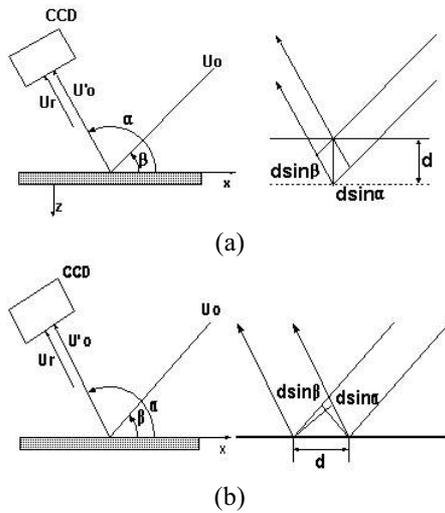
where  $f$  is the number of fringes,  $\lambda$  is the wavelength,  $\alpha$  is the angle of reflection and  $\beta$  is the angle of incidence. So when the angles of reflection and incidence are fixed, the micro deformation is measurable from the number of fringes.[2]



**Fig. 1.** Optical construction of ESPI for (a) out-of-plane and (b) in-plane measurement.

In this study, we tried to apply the ESPI system to measure the micro deformation of the flip-chip during thermal cycling. In order to perform this measurement, improvements were made to the magnification of the ESPI system that is applied to bulk materials, and the thermal deformation at the solder joint in the flip-chip. From these results, the shear strain at this local area was evaluated and these experimental findings verified by

comparison with those obtained by finite element analysis (FEA).



**Fig. 2.** The principle of deformation for (a) out-of-plane and (b) in-plane measurement.

## Experiment

### Improvement of magnification

The ESPI system has the many advantages of being a non-contact, non-destructive, realtime and whole field measurement which allows application during object operation, but it also has a disadvantage of being applicable only to bulk materials because of its resolution. Therefore in this study, long working-distance microscope and zoom lens were attached in front of the CCD camera (Fig. 3) to enable evaluation of the micro device deformation by the magnifying ESPI system.[1]

By adjusting the arrangement of the two lenses, images twenty times larger than previously obtainable were generated and the focus and light intensity could be controlled by the zoom lens and iris. The application of this modified ESPI system may be extended to evaluation of various micro materials, such as microelectronics, the microelectromechanical system (MEMS), and so on, by these magnifying optical arrangements.



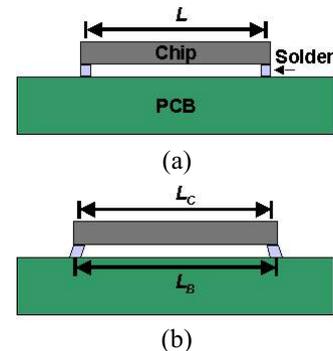
**Fig. 3.** Long working-distance microscope and zoom lens attached to ESPI system.

### Flip-chip solder joint

The improved ESPI system was applied to thermal deformation measurement of the flip-chip, a component widely used in electronic packaging technology.

The flip-chip package is the bonding technology that connects the semiconductor chip on silicon wafer with the printed circuit board (PCB). In contrast to the bonding length dependent time-delay problems associated with wire or lead bonding, flip-chip bonding, featuring the advantages of both volume reduction and performance improvement, is widely used due to its structural simplicity. However, thermal reliability problems occur during operation because it consists of surface joints between materials of different mechanical characteristics, such as the coefficient of thermal expansion (CTE).[3]

A flip-chip consists of chip, PCB and solder joint. The solder joint connects the chip with PCB for electrical, mechanical and thermal purposes. When the operating current generates resistance heat, the package temperature increases and the components undergo thermal deformations (Fig. 4). And due to the CTE mismatch, thermal deformations lead to shear strain at the solder joint. If the current cycles repeatedly, the lifetime of the flip-chip is reduced due to the fatigue failure caused by thermal cycling.[3-5] Therefore by evaluating the thermal deformation appearance of the flip-chip, we attempted to moderate the shear strain arising from the CTE mismatch.



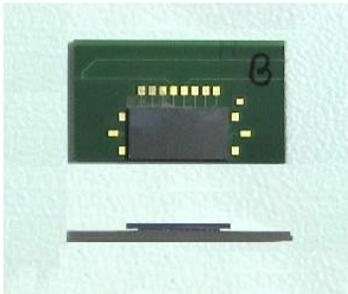
**Fig. 4.** Schematic diagram of the thermal deformation mechanism in the flip-chip package at (a)  $T_0$  and  $T_{max}$ .

### Specimen and thermal vacuum chamber

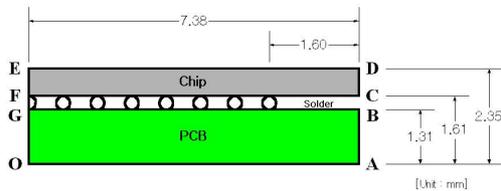
Fig. 5 shows the flip-chip specimen examined in this study. The chip is made by aluminum thin film line on silicon wafer substrate, the under bump metallurgy (UBM) is constructed with copper (2  $\mu\text{m}$ ), nickel (3  $\mu\text{m}$ ) and gold film, and the insulation layer with silicon dioxide ( $\text{SiO}_2$ ). The solder is the widely used Sn-36Pb-2Ag of 500  $\mu\text{m}$  diameter. The chip length and width are 14.82 mm and 8.44 mm, respectively. The right half of the flip-chip was used in this experiment because of its symmetry (Fig. 6). To measure the cross-sectional deformation, the flip-chip was cut. The thicknesses of the chip, solder and PCB were 0.74 mm, 0.30 mm and 1.31 mm, respectively.

A thermal vacuum chamber with optical window was manufactured to model the thermal loading conditions produced by the operating current (Fig. 7). In typical industrial applications the flip-chip is heated up to 125  $^\circ\text{C}$ . [5,6] So in

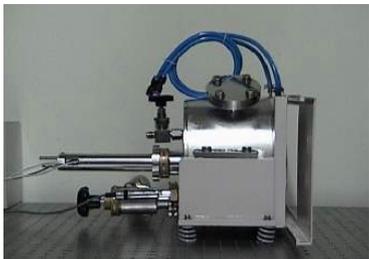
this study, the deformation of the specimen was measured every minute while heating from room temperature (25 °C) to 125 °C at a heating rate of 5 °C/min. An optical window of 210 mm diameter was fitted to the front of the chamber to accommodate the ESPI system. To avoid any alteration in the laser route due to thermal circulation, a vacuum of about  $10^{-3}$  Torr was maintained in the chamber.



**Fig. 5.** Flip-chip specimen.



**Fig. 6.** Flip-chip specimen dimension.



**Fig. 7.** Thermal vacuum chamber with optical window.

## Results and Discussion

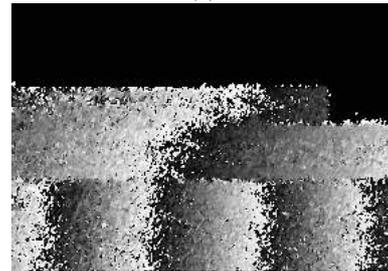
### Thermal deformation measurement

The modified ESPI system was used to non-destructively measure the horizontal displacement of the flip-chip solder joint. Fig. 8 shows the fringe pattern, generated by the speckle interference, which formed along the perpendicular direction to the x-axis because the displacement of the horizontal direction increased as temperature increased. The fringe results confirmed that the number of fringes in the chip and PCB were different, a difference caused by the CTE mismatch effect and which induced the shear deformation at the solder joint connecting the chip with PCB. Fig. 8(d) shows that the fringes became bent from the lower part to the upper part of the solder joint. These observations allowed a rough understanding of the aspects involved in the thermal deformation and a quantitative evaluation of the local displacement of the flip-chip specimen by image-processing technique (Fig. 9). The local displacements of the cross-sectional specimen are indicated with the color images. As

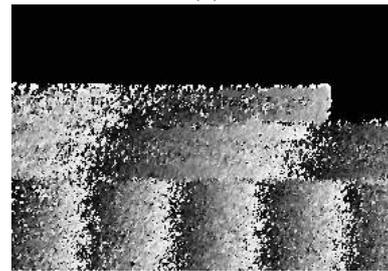
noted above, the fringe observations contributed to an understanding of the effect of increasing temperature on the thermal deformation mechanism. As the deformation is mobile, the stresses were concentrated on the outside of the solder ball, as evident from the color distribution. To calculate the shear strain of the solder joint, the silicon chip and PCB deformations were measured (Fig. 10 and 11). Both the chip and PCB exhibited linear deformations from  $x=0$  mm to  $x=5.78$  mm, displacements where the solder balls were located in an orderly manner because of the restraint force in the linear zone. Beyond  $x=5.78$  mm, nonlinear deformation occurred because the restraint force of the solder joint disappeared. The PCB part was more deformed than the chip part because of the CTE difference. Hence the ability of the ESPI system to measure the local displacement on a sub micrometer scale was clearly demonstrated.



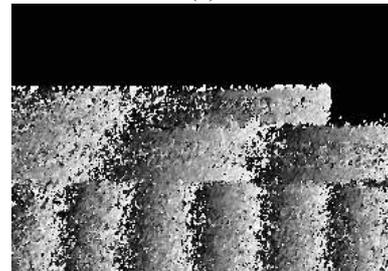
(a)



(b)

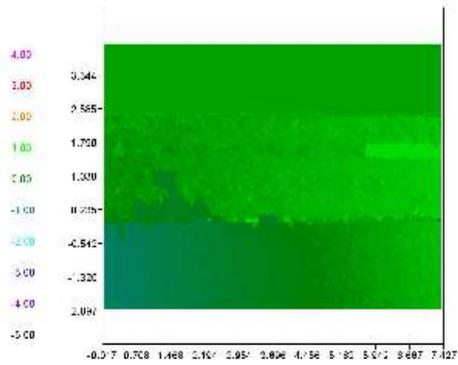


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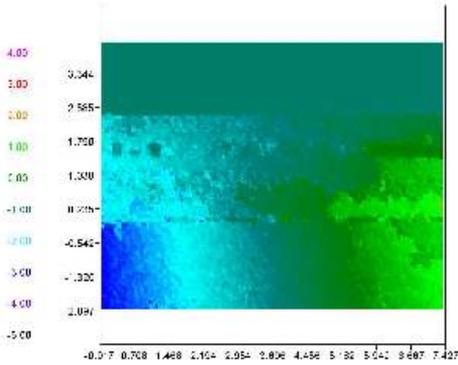


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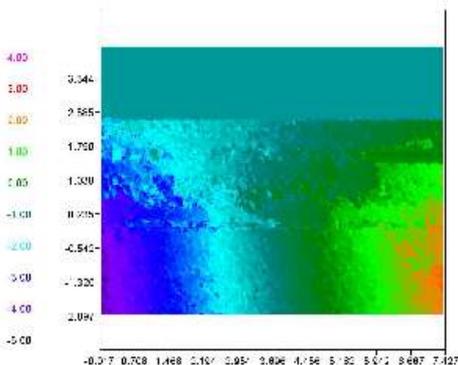
**Fig. 8.** Fringe patterns at (a) 50 °C, (b) 75 °C, (c) 100 °C and (d) 125 °C.



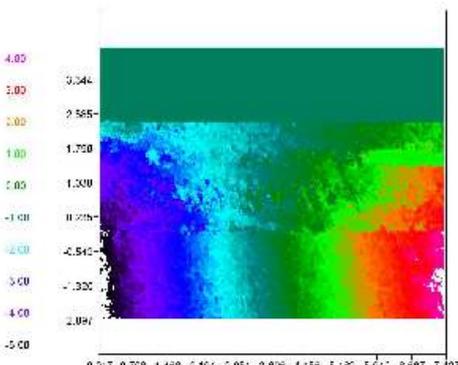
(a)



(b)

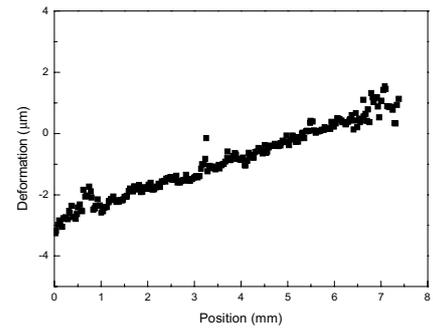


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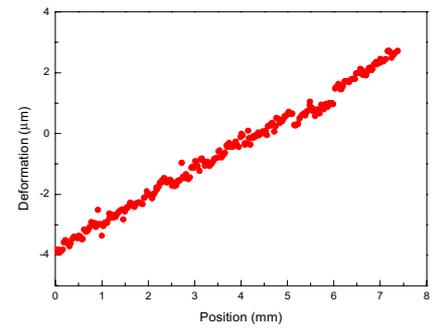


(d)

**Fig. 9.** Deformation images at (a) 50 °C, (b) 75 °C, (c) 100 °C and (d) 125 °C.



**Fig. 10.** Silicon chip deformation at 125 °C.



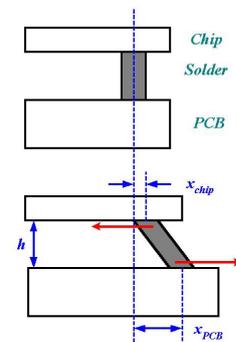
**Fig. 11.** PCB deformation at 125 °C.

Shear strain evaluation

The shear strain of the flip-chip solder joint was calculated from the results obtained by the ESPI system, as shown in Fig. 12. The shear strain  $\gamma$  is given by

$$\gamma = \frac{\Delta x}{h} = \frac{x_{PCB} - x_{chip}}{h} \quad (2)$$

where  $x_{PCB}$  and  $x_{chip}$  are the local displacement of PCB and the chip, and  $h$  is the height of the solder joint. If the center ball is first and the outside ball is eighth, then the eighth solder ball has the maximum shear strain and the outside solder ball is easily generated as a fatigue failure.[3-5] Table 1 shows the shear strains relative to solder joint position and temperature. By determining the shear strain with this method, the lifetime of the flip-chip package can be estimated from the equation predicting fatigue failure.



**Fig. 12.** Shear strain at flip-chip solder joint.

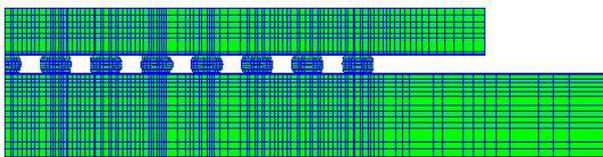
### Finite element analysis (FEA)

To predict the thermal deformation behavior of the flip-chip package and the shear strain of the solder joint, finite element analysis (FEA) was performed. Fig. 13 shows the mesh of the flip-chip for this analysis. A 2D plane strain element was used for the model. Because of symmetry, only one-half was required to be modeled. Elastic behavior was assumed for the chip and PCB, elasto-plastic for the solder joint. There were 4750 plane strain elements and 5053 nodes.[5,6]

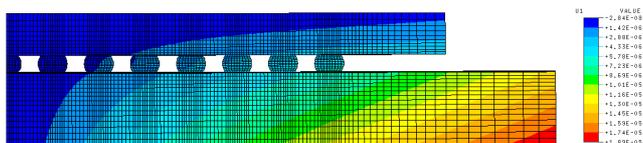
Fig. 14 shows the x-directional displacement over the temperature range 25 °C to 125 °C and confirms that the FEA results are similar those of the ESPI system. In particular, the deformation contours from ESPI and FEA were shown to bend from PCB to the chip because of the restraint force. The shear strains were calculated from the FEA results, and are shown in Fig. 15 along with the ESPI results. As can be seen, the two results correspond well with each other. But we considered that the results in the outside solder ball region weren't in good agreement because of the inherent inaccuracies in the material properties and the FEA assumptions. Other studies [7,8] have shown that the shear strain of the flip-chip solder joint follows a roughly linear relationship. But our result lends support to the validity of this tendency, within experimental accuracies.

**Table 1.** Shear strains at flip-chip solder joint ( $\times 10^{-3}$ )

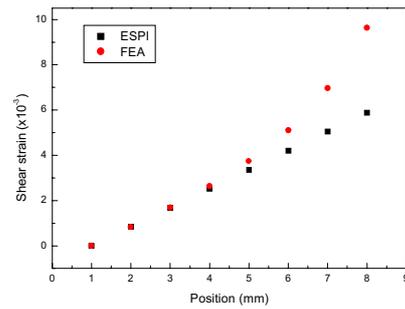
Temp. (°C)	50	75	100	125
1	0	0	0	0
2	0.079	0.28	0.48	0.74
3	0.16	0.57	0.96	1.47
4	0.24	0.85	1.45	2.22
5	0.32	1.13	1.93	2.95
6	0.40	1.42	2.41	3.69
7	0.48	1.70	2.89	4.42
8	0.55	1.98	3.37	5.16



**Fig. 13.** Flip-chip mesh.



**Fig. 14.** Deformation contour from FEA.



**Fig. 15.** Shear strains from ESPI and FEA.

### Conclusions

For application of the ESPI system, previously used for non-destructive measurement of bulk material deformations, to micro devices, we evaluated the thermal deformation of the flip-chip package and obtained the following results:

- (1) The ESPI system, modified with a long working-distance microscope and a zoom lens to improve its resolution, was used to measure the deformation displacement on a sub micrometer scale.
- (2) We measured the thermal deformation of the flip-chip package using this improved ESPI system, and thus were able to locally evaluate each shear strain of the solder joint.
- (3) The experimental results from the improved ESPI system were verified by finite element analysis.

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# Measurement of Thermo-mechanical Deformations of Wafer-Level CSP Assembly Under Thermal Cycling Condition

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## Abstract

The understanding of thermal deformation has been recognized as the key for a reliable electronic packaging design. In this study, thermal deformations of *Ultra* CSP™ 80 assembly during a thermal cycling were investigated using real-time high sensitivity moiré interferometry. For temperature cycling, a small-sized thermal chamber having an optical window was developed. The nominal shear strain of solder joint and the warpage of the wafer-level CSP assembly were measured under a thermal cycle.

## Introduction

As electronic systems get smaller in its size (and coherently, lighter in its weight) and faster in its speed, the packages of microelectronics components rapidly changes to smaller ones, so-called CSPs (Chip Scale Packages). The current TSOPs (Thin Small Outline Packages) are being very rapidly replaced with CSPs in flash memory and SRAM for portable computers and mobile phone applications. The primary driving forces of this transition are its smaller size and lighter weight. In addition, CSPs are superior in electrical performance mainly because their interconnection length is small and, for that reason, undesirable parasitic RLC can be minimized. So, CSPs provide the flexibility in high-speed DRAM application such as Direct RDRAM.

Like the plastic packages such as TSOPs, with the increase of power dissipation and the decrease of package sizes, the heat generated by electric current becomes severe, which will affect the structural integrity and the electrical performance of CSPs. The operating environments also impose stringent requirements on CSPs. According to design requirements, CSPs may be exposed to high and low temperatures ranging from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  in accelerated thermal cycling test. During the thermal cycling test, the CTE mismatch between chip and board is absorbed by the large shear deformation of compliant solder bumps and damage to the solder bumps may readily affect a system's functional integrity. Therefore understanding the thermo-mechanical behaviors and predicting the thermal deformation of CSPs are critically important for the reliability of advanced electronic devices.

Moiré interferometry has been used effectively to measure thermal deformations of electronic package devices. Most of the thermal tests were applied to isothermal loading condition and almost of these experiments were performed for understanding the residual deformation induced by the change of temperature. Recently, several studies using moiré interferometry have been conducted to measure inelastic

deformations accumulated during thermal cycles or time-dependent creep behaviors [1-6]. In this study, the thermo-mechanical behaviors of a wafer-level CSP under a thermal cycle of  $(25^{\circ}\text{C})-(100^{\circ}\text{C})-(0^{\circ}\text{C})-(25^{\circ}\text{C})$  were investigated using real-time high sensitivity moiré interferometry.

## Description of Test Package

The specimen was a wafer-level CSP (Chip Size Package) assembled to an FR-4 PCB [7]. Fig. 1(a) shows a cross-sectional picture of the specimen for moiré interferometry study. One side of the specimen was ground flat to expose the largest cross section of solder bumps for grating replication. The dimensions of the silicon (Si) chip were  $13\text{ mm} \times 6.5\text{ mm} \times 0.68\text{ mm}$  and has 90 I/O interconnections ( $15 \times 6$  solder bump array). The substrate, a FR-4 printed circuit board with copper lines, is 1.5 mm thick.

The chip was connected to a PCB using solder bumps. Fig. 1(b) shows a micro-section of an assembled CSP solder bump. As seen, the gap between the chip and the substrate is  $360\text{ }\mu\text{m}$ , which is also about standoff height of solder bumps. The solder bumps, made of eutectic solder, have a 0.8 mm pitch. The diameter of the bottom surface metallurgy (BSM) pad opening was 0.45 mm, and a copper pad with a diameter of 0.35 mm was used on the PCB side. Dimensions were measured from several micro-sectioned solder bumps. As seen in Fig. 1(b), the solder wets around the copper, creating a wedge shaped section at the bottom.

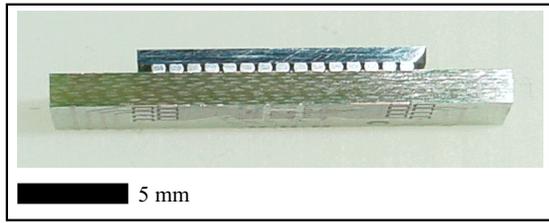
## Experimental Procedure

### *Specimen preparation*

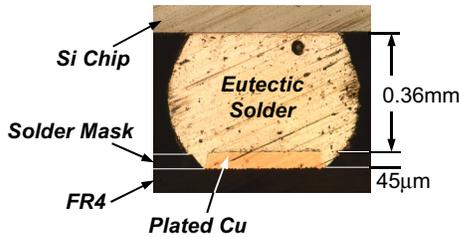
Moiré interferometry requires a plane of interest to be revealed and ground flat before specimen grating replication. A specimen was cut into rough dimensions using a high precision diamond wheel saw. The specimen was inserted in a small-sized precision vise. Then the specimen surfaces were ground with coarse sandpapers and polished by #2000 fine sandpapers. The surface was then cleaned with ethanol and dried thoroughly. Before the moiré measurement, the specimen was kept in deccigator for 2 days to remove the moisture from the package.

One of the most important parts of this experiment was selection of the epoxy. A proper type of epoxy was chosen after many trial and errors to make sure that the specimen grating would stand the peak cycling temperature for many

times. In addition the viscosity of the epoxy should be extremely low for a very thin layer as it was spread out on the specimen surface to replicate the grating. The high-temperature-curing epoxy (F253, TRA-BOND) was used for this experiment. The grating replication procedure was performed at room temperature (25°C). The epoxy was cured during about 7 days at room temperature. The high-frequency(1200 lines/mm) crossed-line diffraction grating was used. So the frequency of a virtual reference grating is 2400 lines/mm and the sensitivity of a displacement measurement is 0.417 μm/fringe order.



(a)



(b)

Fig. 1 Specimen for moiré interferometry study: (a) Specimen cut from CSP assembly, providing cross section having 15 solder bumps; (b) Cross-section of the solder bump of CSP assembly.

*Thermal loading condition and experimental setup*

Real-time measurement technique was used to measure the deformations of solder joints and the relaxation of warpage induced by temperature changes. The temperature history used in the experiment is shown in Fig. 2. The environment chamber and support carriage were used with a four-beam moiré interferometry system (PEMI; Portable Engineering Moiré Interferometer from Photomechanics) to acquire *in-situ* deformation patterns as a function of temperature and time in a controlled environment. Fig. 3(a) shows the experimental setup schematically. The fringe patterns were recorded by a CCD camera system or a large format camera system.

For *in-situ* or real-time measurement of the thermal deformations, a small-sized thermal chamber having an optical window was developed (shown in Fig. 3(b)). The conduction heating and cooling scheme using tape-type heaters and thermoelectric(Peltier) modules was applied to the chamber.

The instrument can be used for the study of the behaviors of packaging structures at the temperatures ranging from -10°C to 180°C. Stable temperature can be achieved with 1°C maximum variation by the method of closed loop control, even for long time creep testing. Also this chamber can be used for the simulation of a accelerated thermal cycling test. The heating and cooling capacity is up to 200°C per 15 min.

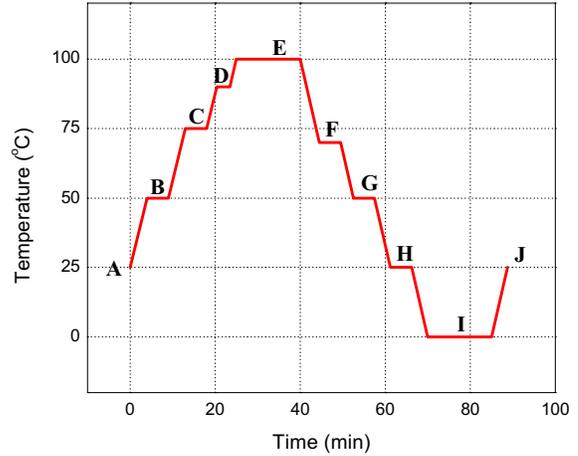
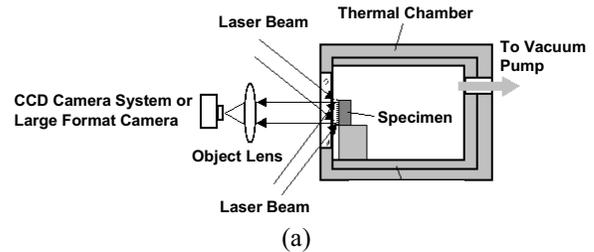
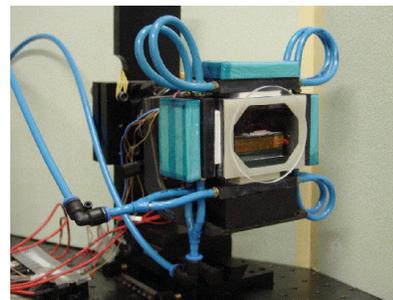


Fig. 2 Temperature history used in the moiré measurement.



(a)



(b)

Fig. 3 *In-situ* or real-time moiré interferometry system: (a) Schematic drawing of the test setup; (b) Small-sized thermal chamber with optical windows.

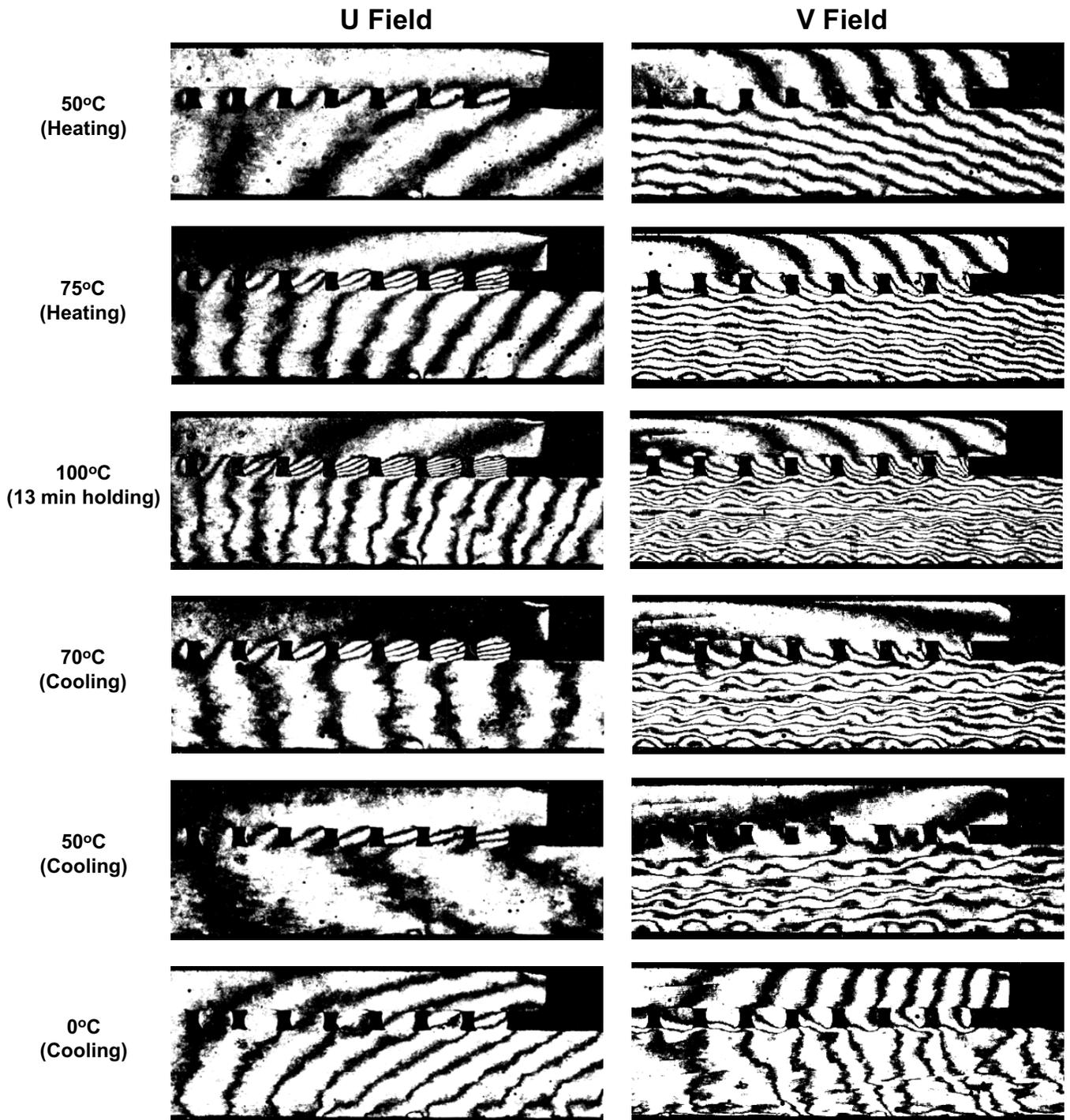


Fig. 4 Moiré fringes of the right half of the wafer-level CSP assembly induced by temperature changes.

## Test Results and Discussions

### *Nominal shear strain of the solder joints*

Fig. 4 show the displacement fields of the right half of the specimen obtained from the real-time moiré measurement corresponding to the temperature changes in Fig. 2. In the x-direction, the CTE mismatch resulted in different

displacements in the chip and the board. Their relative displacement at any point is a function of the distance from that point to the geometric center of the assembly. At the ends of the chip, the relative displacement reaches its maximum value, which cause the highest strain in the rightmost solder bump. Fig. 5 shows the magnified view of the U displacement fringe patterns of the rightmost solder joint. As shown in Fig.

5, the relative displacement was linearly distributed over the height of the solder joint at all stage of the temperature, which indicated a uniform shear strain in the interconnection.

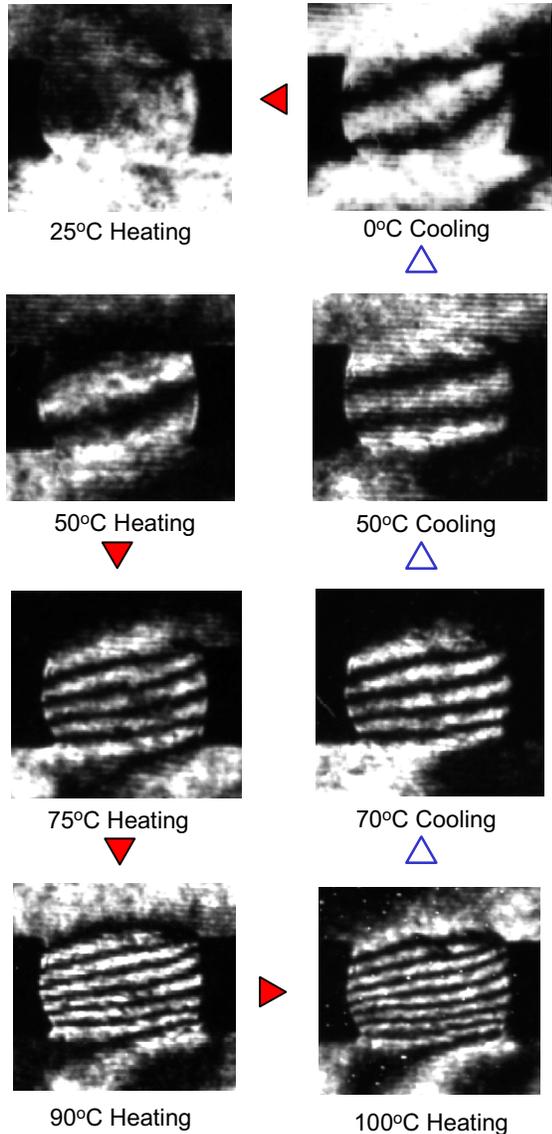


Fig. 5 U displacement fields of the rightmost solder joint.

By using the U field fringe patterns as shown in Fig. 4 and Fig. 5, the relative displacement in the x direction between the two surfaces (the bottom surface of the chip and the top surface of the board) can be determined. The nominal shear strains in the solder joints can be also calculated by dividing the relative displacement at that position (the centerline of the solder bump) by the standoff-height of the solder bumps (about 360  $\mu\text{m}$ ). Fig. 6 shows the nominal shear strains of the rightmost solder joint corresponding to the temperature.

During the heating process, the nominal shear strain in the joints increased nonlinearly because of the creep behavior of the eutectic solder and it reached its maximum value at 100°C (about -0.9 %). It returned to almost zero when the assembly was cooled to room temperature. The shear strain with an opposite sign was developed when the temperature was decreased to 0°C and it reached its maximum value at 0°C (about 0.2%). But during the cooling, the shear strain decreased almost linearly, which indicates that temperature-dependent nonlinear behavior is much less significant during the cooling process. In the case of CBGA assembly, it is reported that the creep shear strain of the eutectic solder fillet produced at the maximum temperature was not recovered during cooling [2]. This behavior is just opposite to that of the solder joints of this wafer-Level CSP. On the contrary, the behavior of the solder joints is similar to that of solder ball of the CBGA assembly.

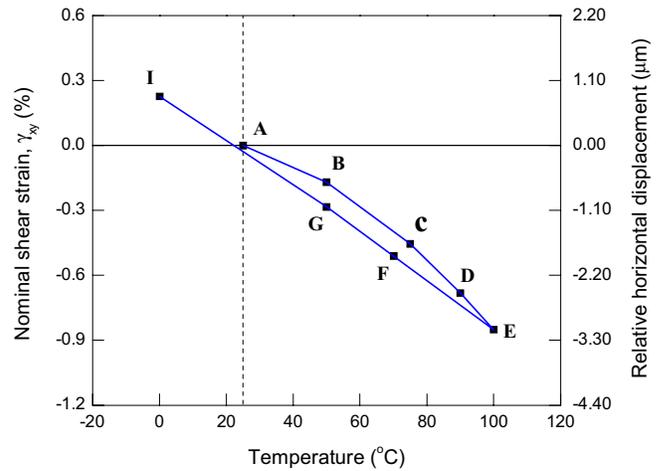


Fig. 6 Nominal shear strain history of rightmost solder joint.

#### Bending behavior(Warpage) of the chip

The chip and board also bent as one can see from the inclined fringes in the U displacement field. During the heating process, the bottom surface of board expanded more than the top, indicating the bend of the upward direction. The V displacement field fringe patterns were analyzed to obtain the bending displacements induced by temperature changes along the centerline of the chip. The results are shown in Fig. 7. Fig. 8 shows the maximum bending displacement of the chip corresponding to the temperature. When the assembly heated to 50°C, the bending displacement increased linearly. The bending displacement increased as the temperature was increased to 75°C. However, the bending displacement decreased when the further increased to 100°C. This phenomena is caused by the creep and stress relaxation of the solder joints. During the cooling process, the assembly bent in

the opposite direction(downward). As shown in Fig. 7, the magnitude of the bending displacement decreased linearly as the temperature decreased and the thermal cycle produced a residual downward bending deformation. These trends are almost same results as those of the CBGA assembly.

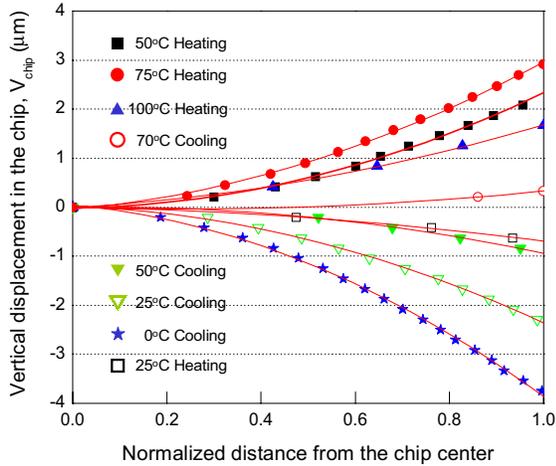


Fig. 7 Vertical displacement distributions along the centerline of the chip

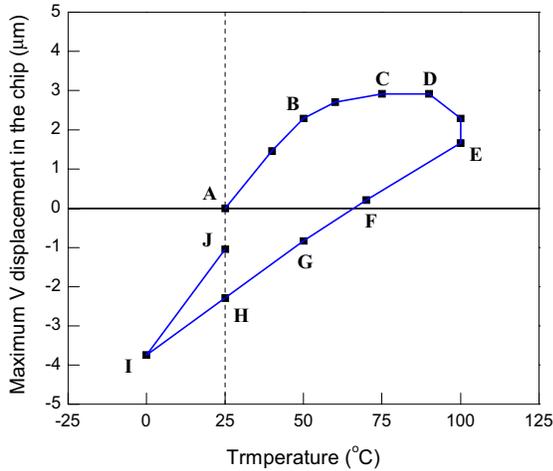


Fig. 8 Maximum bending displacement of the chip corresponding to the temperature.

## Conclusions

To investigate the thermal deformations of the wafer-level CSP assembly during temperature cycling, real-time measurement technique was used to measure the deformations of solder joints and the relaxation of warpage during a thermal cycle of (25°C)-(100°C)-(0°C)-(25°C). For *in-situ* or real-time

measurement of the thermal deformation, a conduction type small-sized thermal chamber having optical window was developed using tape-type heaters and thermoelectric(Peltier) modules. The results indicated that the nonlinear thermal deformations during heating were caused by the creep and stress relaxation of the solder joints. But the thermal deformations of the assembly during cooling showed the linear behavior, which indicates that temperature-dependent nonlinear behavior is much less significant during the cooling process. It is interesting to note that the shear strain of the solder joint was recovered during cooling process.

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