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Thermal and Moisture Induced Stressing Effects of RF Power Amplifier Modules

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Abstract

Underfill delamination analysis of flip chip on low-cost board is presented in this study. The delamination propagation rates at the interface between chip and underfill have been measured by using C-SAM inspection of flip chip assemblies under thermal cycle loading. The experimental measurement was done in 4 cases, that were type B with fine solder joint and fractured solder joint, and type D with fine and fractured solder joint. In the finite element simulations related, the strain energy release rates G and the phase angles φ near the delamination crack tip were calculated for 4 measurement cases by employing the fracture mechanical method. The Paris half-empirical equation were determined from the delamination propagation rates measured and the energy release rates simulated. The energy release rates G with different delamination crack length a were also simulated. The $G \sim a$ curve represents a convex shape when the crack propagates and indicates that the delamination crack may be stable and after propagating a certain length the crack will be arrested in flip chip assembly.

1. Introduction

The use of direct chip attachment technologies, such as chip-on-board (COB), chip-on-glass, and flip-chip (FC) designs enables one to eliminate one level of device packaging in IC packaging industry [1]. Due to the high input/output (I/O) density, low-cost assembly, and low "package" profile, it is expected, that the flip-chip technology will become a mainstream technology in the future [2,3]. In order to release thermal mismatch during flip chip package operation and improve the long term reliability of flip-chip, a rigid underfill has been applied to fill the gap between the chip and the organic substrate as an effective solution [4]. It is reported by Nakano et al. [5] that certain polymers such as epoxies heavily filled with particles of SiO_2 between the chip and substrate will increase the fatigue life of the solder joint by a factor of 10-100 in 1987. In 1994, it is found that the packages are almost the same reliability when employing epoxy resin filled between chip and FR4 substrate, comparing with using ceramic substrate only by Tsukada [6].

A number of experimental measurements have been reported in recent years. C.K.Gurunmurthy et al. [7] applied a noncontact fiber optic displacement sensor to investigate the crack growth rate (da/dn) along underfill/metal interface under thermal fatigue condition in 1998. S.Y. Kook et al. [8] used four-point bend bars to characterize delamination propagation behavior at the interface between polymer and metal. Both of them analytically calculated the strain energy release rates G near the crack tip under different conditions in their researches and obtained their relations between G and da/dn . In the same

year, Sheng Liu et al.[9,10] experimentally measured the interfacial fracture toughness of chip/underfill interface with three-point bending and C.P. Wong et al. [11] measured the apparent fracture toughness of the interfaces between epoxy-based underfill materials and various substrates. Recently, Lau et al.[12] investigated modes of delamination propagation with a case study of finite element simulations in flip chip package.

In this paper, the delamination propagation behavior at the interface between chip and underfill was analyzed both by experimental measurement and finite element simulation and the half-empirical Paris equation was determined.

2. Experimental Methodology

2.1 Samples and tests

Two types of test chip (type B and D) were used in the experiments. The test chips, which had alternate pads connected to form a daisy chain structure, were fabricated by Flip chip Technology, Co., Ltd. The dimension of the test chip B is $5.6 \times 6.4 \text{ mm}^2$, with 96 peripheral eutectic SnPb solder bumps on a pitch of $203 \mu\text{m}$ and the dimension of the test chip D is $6.3 \times 6.3 \text{ mm}^2$, with 48 peripheral eutectic SnPb solder bumps on a pitch of $457 \mu\text{m}$. FR4 printed circuit boards with Cu pads coated with a Ni/Au layer was used as the substrate. Assembly was performed by using a no-clean flux LR721H₂BGA. The solder joints were formed by an IR reflow soldering process with a typical temperature profile having a peak temperature of 230°C . Underfill was performed at $60^\circ\text{C} - 70^\circ\text{C}$ from one side of the chip in $\sim 20\text{s}$ and cured at 150°C for 20 min.

After underfilling, the samples were tested in a thermal cycling chamber. The thermal cycling testing followed MIL-STD-883C. The temperature of thermal cycling ranged from -55°C to 125°C with a dwell time at each temperature of 30 min. And the changeover time was less than 10s. In *situ* temperature measurements indicated that the new temperature achieved in about 5 min. Then after each changeover electrical continuity and C-SAM checks were performed approximately every 200 cycles. A SONOSCAN D6000C-SAM with a 230 MHz transducer was used for the acoustic microscopy. Some typical samples were selected for cross sectioning and investigation by optical and scanning electron microscopy (SEM).

2.2 Experimental determination of solder joint states

It is verified by our pervious experimental research that C-SAM is not only sensitive to underfill delamination of flip-chip assembly but also can be used to evaluate solder's fatigue degree of solder joints [13]. Figure 1(a) and 1(b) show the C-SAM images of typical sample with underfill before and after thermal cycling, respectively. It can be seen from Figure 1(a)

that there was no delamination or voids in the underfill before the thermal cycling test. The uniform contrast in the acoustic image of the solder joints indicates the good integrity of solder joints. However, the acoustic image of the same sample after 772 thermal cycles in Figure 1(b) shows the different acoustic contrast in different solder joints. Some solder joints had become brighter (arrow D2) than the others (arrow D1) and those bright solder joints tended to become much bright as the thermal cycling test proceeded. Our previous work [13] indicates that this acoustic contrast variation can be associated with the occurrence of defects in the solder joint. In order to identify the defects which occurred in the solder joints, a number of samples were analyzed by cross sectioning and the cracks were found in those solder joints with a higher acoustic contrast, while no cracks were found in the solder joint with normal acoustic contrast.

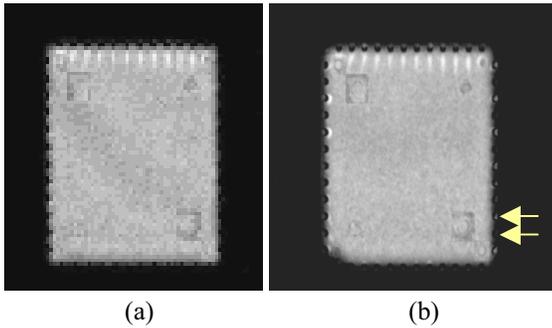


Fig.1 (a) Acoustic image of a typical sample with underfill before thermal cycling, showing the good integrity of solder joints; (b) Acoustic image of the same sample after 772 thermal cycles, showing different acoustic contrast in different solder joints

Figure 2 shows the SEM images of two solder joints with different contrasts corresponding the solder joint D1 and D2 in Figure 1. The SEM image in Figure 2(a) shows no cracks were found in the solder joint D1 with normal acoustic contrast and the SEM image in Figure 2(b) indicates a through crack was found in the solder joint D2 with brighter acoustic contrast. This experimental result verified that C-SAM measurements do provide convincing information for qualitative determination of the crack state (the crack occurred or not in the solder joint) of the flip chip assembly tested. From this correlation, it can be concluded that the higher acoustic contrasts are corresponding the solder joint

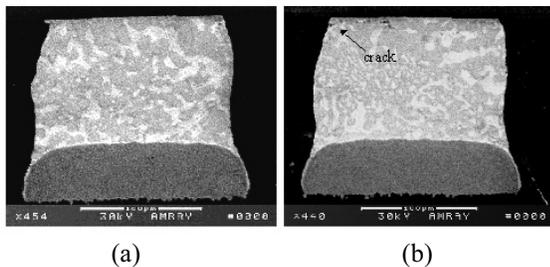


Fig.2 (a) SEM image of a joint with normal acoustic contrast in Fig. 2 (arrow D1) showing no cracks were found; (b) SEM image of a joint with brighter acoustic contrast in Fig. 2 (arrow D2) showing a through cracks were found in the solder joint

with crack and the normal acoustic contrasts are reflecting the solder joint without crack.

This result gives a possibility to measure two delamination crack growth rate (da/dn) in chip/underfill interface for two states of solder joint (with and without crack in solder joint itself, i.e., fine solder joint case and fractured solder joint case).

2.3 Experimental determination of delamination growth rate

After every additional approximately 200 cycles in the thermal cycle testing, the samples were inspected by C-SAM and the chip area delaminated were measured by special software to evaluate delamination degree. The corresponding mean crack lengths as thermal cycle processing were calculated and presented in Figure 3 for type D. The slopes of the straight line in Figure 3, da/dn , are listed in table I for type D and B assemblies, and for solder joint with and without crack. From table I, it was revealed that the delamination cracks in chip/underfill interfaces for fine solder joint case were propagating faster than those for fractured solder joint case.

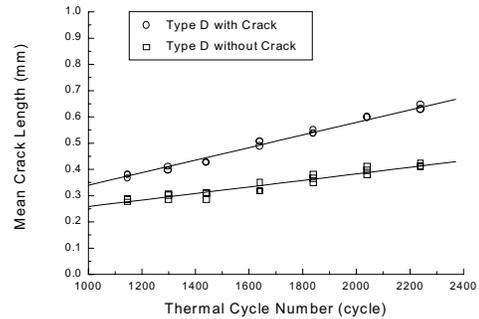


Fig.3 Dependence of delamination crack length on the number of thermal cycles for samples of type D

Table I Crack growth rate da/dn of solder joint with and without crack (unit:mm/cycle)

case	da/dn
B type solder without crack	0.000215
D type solder without crack	0.000114
B type solder with crack	0.000248
D type solder with crack	0.000257

3 Finite Element Analysis

3.1 Finite Element modeling

In this study, the variation of displacement field has been simulated under the thermal cycling loading. The simulation method is the same as the thermomechanical behavior simulation in our pervious work and can be found in elsewhere [15,16]. All FE analysis in this study was simulated from 2D models and the plane strain condition was adopted in present simulations. Due to symmetry, only half of the 2D model was meshed. A 2D structure containing a pre-crack on the interface between the chip and underfill in flip chip assembly was established as shown in Figure 4. A corresponding FE mesh of D type of flip chip assembly is

shown in Figure 5. In order to calculate the near-tip displacement field, the local fine mesh was processed near the delamination crack tip on the interface between chip and underfill. In the present FE model, a crack with experimental measured mean crack length was pre-located in the interface. The contact element in ANSYS, CONTEC48, was installed at certain critical locations on the delaminated surface.

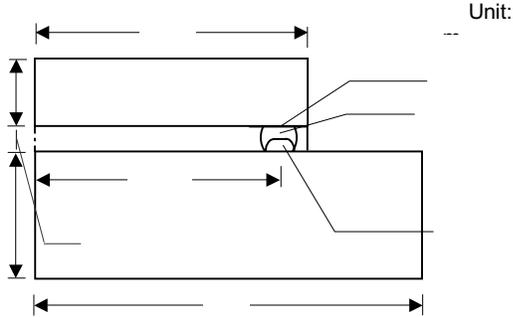


Fig.4 Schematic 2D structure containing a pre-crack on the interface between chip and underfill in flip chip assembly

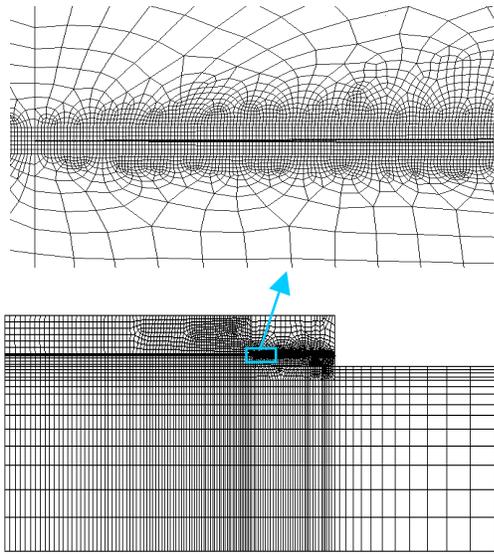


Fig.5 FE mesh of D type of flip chip assembly containing a pre-crack on the interface between chip and underfill

Table II Material properties for FE modeling

Materials	E (GPa)	α (ppm/°C)	ν
Silica	131	2.7	0.3
FR4	16	16	0.28
Copper	120	17	0.35
60Sn40Pb	30.685-0.993T	25	0.35
Underfill	9(LT)~0.3(HT)	26(LT)~110(HT)*	0.3

* LT low temperature; HT high temperature

The material properties of SnPb eutectic solder used in the present simulation were following the Anand viscoplastic material model, and the Anand material parameters fitted by us [17,18] was used. The Young's modulus of solder 60Sn40Pb are temperature-dependant, meanwhile for underfill U8437-3, not only the Young's modulus but also the

coefficients of thermal expansion are temperature-dependant, and the details can be found in our pervious publications [16]. Table II gives the elastic material properties of related materials used in the simulations (Young's modulus, coefficients of thermal expansion, and Poisson ratios). The thermal cycle loading condition in this FE simulation was from 125°C to -55°C, and a stress-free status was assumed at the high temperature $T=125^\circ\text{C}$.

3.2 Fracture Mechanics Methodology

Interfacial fracture mechanics is an important approach for characterizing material resistance to interfacial delamination failure and for making interface reliability prediction. A half-empirical equation, Paris equation as following can give the correlation between delamination propagation rate da/dn and energy release rate range ΔG ,

$$\frac{da}{dn} = A(\Delta G)^m \quad (1)$$

The relationship between da/dn measured and ΔG simulated is very useful for the predicting delamination crack propagation and the optimum design of flip chip packages by modeling with finite element analysis.

3.2.1 J-integral method

For uniform material, the J-integral near the crack tip in fracture mechanics is a critical variable and its value is path-independent. In terms of the strain energy density $W(=\sigma_{ij}\epsilon_{ij}/2)$, the stress field σ_{ij} and the displacement field u_i , the J can be expressed as follows:

$$J = \int_{\Gamma} (Wn_x - T_i \frac{\partial u_i}{\partial x}) ds \quad (2)$$

where Γ is a path of arbitrarily chosen contour which begins at any point on the lower crack surface, encircle the tip, and ends at any point on the upper crack surface; and n_i is the unit outward normal to Γ . T_i is the force along the integral path ds. For uniform linear elastic material, the J-integral is the same as the energy release rate G. However, for the crack in the bimaterial interface, the value of J-integral would be not rigorous path-independent. However, due to that the necessary of comparison with other variables calculated, the J-integrals with FE modules were also calculated in this work.

3.2.2 Straightforward method

By definition, G is the change of strain energy release per unit crack growth. By running two analyzes with a small increment in crack length $\bullet a$ and evaluating the total strain energy of each case, the value of G can be calculated by following expression

$$G = -\frac{U_{a+\Delta a} - U_a}{B\Delta a} \quad (3)$$

where B is the thickness of sample and can taken as $B=1$ in 2D simulation. U is the total strain energy. The straightforward method is quite obvious in physical meaning, but the computational time would become double. Moreover, because $\bullet a$ is so small that the difference $(U_{a+\Delta a} - U_a)$ from a great quantity to substrate another great quantity could result in a loss of computational precision seriously.

3.2.3 Crack tip opening displacement (CTOD) method

According to the displacement variations near the crack tip both in crack opening direction and shearing direction, the crack tip opening displacement method can be used for calculating the complex stress intensity factors (real part K_I for opening mode; image part K_{II} for shearing mode) and then the strain energy release rate G and phase angle φ can be obtained. The displacement fields near crack tip that can be obtained through either experimental method such as micromoire interferometry or numerical calculation such as the finite element analysis. In this work, a commercial finite element code, namely, ANSYS, is employed to determine the near tip displacement fields. Based on results from FE simulation, the energy release rate G and phase angle φ were calculated by using the equation set given by S. Liu et al.[10] recently:

$$G = \frac{1}{4} \left[\frac{D_{11}}{\cosh^2 \pi \varepsilon} K_I^2 + \left(D_{11} - \frac{W_{21}^2}{D_{11}} \right) K_{II}^2 \right] \quad (4)$$

$$\varphi = \tan^{-1} \frac{K_{II}}{K_I} \quad (5)$$

The above parameters D_{11} , K_I , K_{II} , W_{21} and ε are defined as follows:

$$D_{11} = \frac{1-\nu_1}{G_1} + \frac{1-\nu_2}{G_2} \quad (6)$$

$$K_I = \frac{\Delta u_1 I_m(\zeta_2) + \Delta u_2 Re(\zeta_2)}{I_m^2(\zeta_2) + Re^2(\zeta_2)} \frac{1}{D_{11}} \sqrt{\frac{\pi}{2r}} \quad (7)$$

$$K_{II} = \frac{\Delta u_1 Re(\zeta_2) + \Delta u_2 I_m(\zeta_2)}{I_m^2(\zeta_2) + Re^2(\zeta_2)} \frac{1}{D_{11}} \sqrt{\frac{\pi}{2r}} \quad (8)$$

$$W_{21} = \frac{1-2\nu_1}{2G_1} - \frac{1-2\nu_2}{2G_2} \quad (9)$$

$$\varepsilon = \frac{1}{2\pi} \ln \frac{G_1 + G_2(3-4\nu_1)}{G_2 + G_1(3-4\nu_2)} \quad (10)$$

The parameter ζ_2 is of the form

$$\zeta_2 = \frac{1}{(1+4\varepsilon^2)\cosh \pi \varepsilon} \left(1 - 2i\varepsilon \left\{ \cos \left[\varepsilon \ln \left(\frac{r}{2a} \right) \right] + i \sin \left[\varepsilon \ln \left(\frac{r}{2a} \right) \right] \right\} \right) \quad (11)$$

where Δu_1 , Δu_2 stand for the near-tip displacement field in both opening and shearing directions, respectively. G_1 and ν_1 represent the shear modulus and Poisson ratio of material I, respectively. G_2 and ν_2 are representative of the shear modulus and Poisson ratio of material II, respectively. It can be seen from Eq. (4) to Eq. (10) that the energy release rate and phase angle used in this study are only the near tip displacement-based functions. That is, the energy release rate and phase angle can be easily be calculated from Eq. (4) to Eq. (10) if the near tip displacement fields are determined. The phase angle in Eq. (5) reflects the dominate kind of fracture mode (opening mode if $\varphi < 45^\circ$; shearing mode if $\varphi > 45^\circ$).

3.3 Energy release rates and phase angles

The results of ΔJ and ΔG in thermal cycling from above three methods are presented in Table II and the phase angles φ from the CTOD method are listed in Table III. It can be seen from the Table II that the values of energy release rates ΔG from the straightforward and CTOD method are approximately equal and the relative error is less than 7%, which indicates that both methods can be used for calculating of ΔG . Meanwhile, the values of ΔJ are also closed the values of ΔG from both methods, showing that all the three methods

are useful and the results are convincible.

It can also be found from the Table III that the ΔG calculated from the models with crack in solder joints are larger than those from the models without crack in solder joints. This is because there is no mechanic coupling from solder joints in the case with crack in solder joint and the delamination will grow faster than in the case without crack in solder joint, coinciding with the experiment measurements from the C-SAM inspections. In the case with crack in solder joint, the values of ΔG for both type B and D are closed, and the delamination propagation rates are also closed. However in the case without crack in solder joint, ΔG values for both B and D types is quite different. In the fine solder joint case without crack, the ΔG for type D is much smaller than those for type B and the crack propagation rates for type D is much slowly than those for type B. It may be resulted from that the standoff height of D type assembly (112 μm) is higher than that of B type assembly (94 μm). The underfill in D type assembly is thicker and will give more mechanic coupling than that in B type. From Table IV, the phase angles φ for all cases are about 55° and the differences are not large, showing the shearing mode is dominant and the fracture behaviors are similar for both B and D types with and without crack in solder joint.

Table III ΔG and ΔJ calculated by three methods from the simulations (J/m^2)

	B, solder without crack	D, solder without crack	B, solder With crack	D, solder with crack
CTOD	18.9	7.8	26.5	27.9
straightforward method	19.6	8.4	25.9	26.5
J-integral	17.8	7.8	28.5	26.2

Table VI Phase angle (degree) calculated by CTOD method from the simulations

	B, solder without crack	D, solder without crack	B, solder with crack	D, solder with crack
CTOD	52.7	54.8	57.6	57.5

4. Results and Discussion

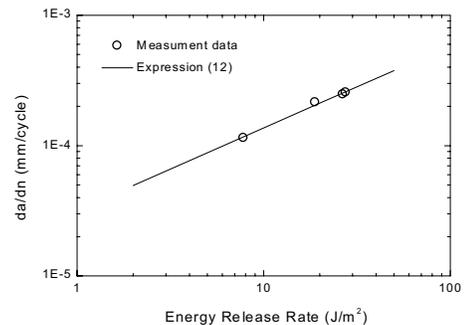


Fig.6 Delamination propagation rate da/dn and energy release rate ΔG of flip chip assemblies tested

Figure 6 shows the delamination propagation rate da/dn from the experimental measurements and the ΔG from the FE simulations with CTOD method for flip chip assemblies tested. A good linear relationship among them can be found and the Paris half-empirical Eq. (1) can be created with the material constant $A = 3.10 \cdot 10^{-5}$ and $m = 0.64$:

$$\frac{da}{dn} = 3.10 \cdot 10^{-5} (\Delta G)^{0.64} \quad (12)$$

Figure 7 gives the results of $da/dn \sim \Delta G$ in this work and the comparison between our data and thermal cycle fatigue results by C.K.Gurumurthy et al. [7] together with the mechanic cycle fatigue data by S-Y Kook et al. [8].

The delamination crack propagation along the interface of underfill/polyimide passivation under thermal cycle loading was measured by Gurumurthy et al. The value of $m=1.37$ in their Paris equation is twice larger than $m=0.64$ in our work, while their phase angle $\phi=58^\circ$ is similar to $\phi \sim 55^\circ$ in this work. A reason for the lower value of $m=0.64$ in this research is that the solder joints are located peripherally on the test chips. When crack propagating, a crack length increase da will result in a delamination area increase by a factor of square.

The delamination propagation rates along the interface between polymer (Phenol-Novolac)/Cu coating with Ni was measured by S-Y Kook et al. They reported that the $\log(da/dn) \sim \log(\Delta G)$ relationship was similar to a sigmoidal curve. Our result from measurements and simulations is closed to the middle part of and a convex shape of $G \sim a$ curve (see Fig.7).

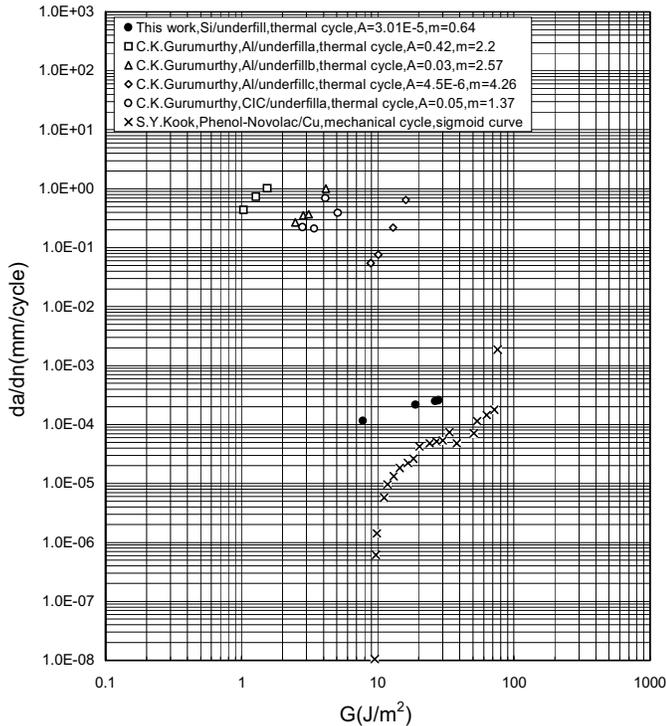


Fig.7 Crack propagation rate from experiment and G by calculation

Recently, Lau et al. [12] have pointed out that there are two basic modes of the delamination crack propagation in flip chip assembly. In the first mode, the strain energy release rate G will always increase with respect to the crack growth. This is an indication of unstable delamination crack and will lead to catastrophic failure. In the second mode, the $G \sim a$ curve represents a convex shape when the crack propagates. This indicates a stable delamination crack and the crack will be arrested (stop) after propagating a certain length. In Figure 7, the values of da/dn measured from different authors under the same G value show a variation with 3~4 orders of magnitude, that may be due to the different modes of the delamination crack propagation in flip chip assembly.

Up to our knowledge, the Paris half-empirical equation fitted from da/dn measured by C-SAM and G simulated by FE analysis have not been reported for real flip chip assemblies under thermal cycle loading. The lower value of $m=0.64$ may be reasonable and the result in this work may be useful practically since the experiment method in this work is close to the real working condition of flip chip packages. The Paris equation from this work can be used as a design base of flip chip package reliability.

In this work, the G with different delamination crack length were also calculated (Fig. 8). The $G \sim a$ curve represents a convex shape when the crack propagates and indicates that the delamination crack may be stable and after propagating a certain length the crack will be arrested in flip chip assembly.

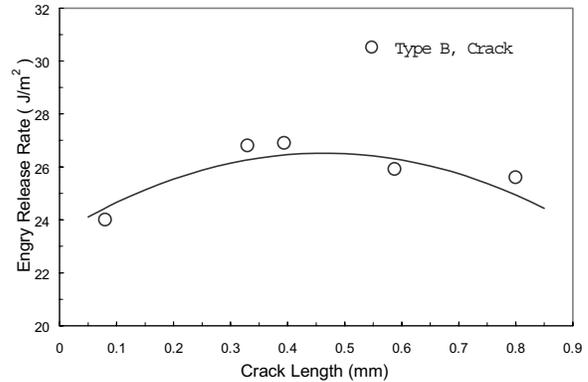


Fig.8 Energy release rate G and crack propagation length a

Many authors determined experimentally the fracture toughness G , although they did not measure the crack propagation rate. It is a matter of great significance to compare our simulated G with their experimental fracture toughness. In the research of S. Liu et al.[10], the interfacial fracture toughness $G=35 \text{ J/m}^2$ and phase angle $\phi=65^\circ$ for three-point bending flip-chip specimen with crack length of 4.5mm were obtained for interface Si/underfill, respectively. C.P. Wong et al.[11] applied four-point bending test to measure the apparent interfacial toughness of the interfaces between epoxy-based underfill materials and various substrates including Al, polyimide, BCB and FR-4 with solder mask and the apparent interfacial toughness 34J/m^2 , 48J/m^2 , 35J/m^2 , and 50J/m^2 were determined

respectively. The above interfacial toughness is higher than the energy release rate G from our simulations, indicating the delamination will not occur in early stage of thermal cycling. This is consistent with the experimental results from the C-SAM measurements. Whereas accompanying with thermal cycle course, the interfacial toughness of underfill/chip interface will degraded gradually and the crack initiation and delamination propagation will happen at a certain cycle period. The C-SAM observation reflected this failure progress of flip chip assemblies in the test.

5. Summary

In this study, the delamination propagation behavior at the interface between chip and underfill were studied and the crack propagation rates were measured by using C-SAM inspection under thermal cycle loading. The strain energy release rates G and the phase angles φ under different conditions were calculated by employing the fracture mechanical method from the finite element simulations related and the Paris half-empirical equation have been determined from the crack propagation rates measured and the energy release rates simulated.

Acknowledgments

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Reliability Evaluation and Failure Analysis for High Voltage Ceramic Capacitor

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Abstract

This paper presents a result of failure analysis and reliability evaluation for high voltage ceramic capacitors. The failure modes and failure mechanisms were studied in two ways in order to estimate component life and failure rate. The causes of failure mechanisms for zero resistance phenomena under withstanding voltage test in high voltage ceramic capacitors molded by epoxy resin were studied by establishing an effective root cause failure analysis. Particular emphasis was placed on breakdown phenomena at the ceramic-epoxy interface. The validity of the results in this study was confirmed by the results of accelerated testing. Thermal cycling test for high voltage ceramic capacitor mounted on a magnetron were implemented. Delamination between ceramic and epoxy, which might cause electrical short in underlying circuitry, can occur during curing or thermal cycle. The results can be conveniently used to quickly identify defective lots, determine B_{10} life estimation each lot at the level of inspection, and detect major changes in the vendors processes. Also, the condition for dielectric breakdown was investigated for the estimation of failure rate with load-strength interference model.

1. Introduction

High voltage ceramic capacitors molded by epoxy resin (called later HV ceramic capacitor) are widely used in power electronic circuits, such as filters, snubbers, and resonant circuits, due to their excellent features of stability and good electrical performance. Despite these benefits, HV ceramic capacitors are generally not used in high voltage applications because of their perceived lower reliability. This is because the dielectric breakdown strength of HV ceramic capacitor is low. Several investigators [1]-[5] have conducted detailed studies to understand the causes and mechanisms of these failures. Although there has been significant improvement for the quality and reliability of HV ceramic capacitors over the last decade, electronic industry's experience is that this problem has not been fully eliminated. Even though adhesive material development and manufacturing techniques have been achieved to some extent, failure mechanisms have prevented widespread use of HV ceramic capacitors, and are not well understood. If failure mechanism for HV ceramic capacitors are better understood, the capacitor's reliability for more severe conditions such as high temperature or high voltage can hopefully be established. Therefore, it is necessary to understand the HV ceramic capacitors failure mechanisms in order to devise improvement in either the material compositions or processing techniques.

Failure analysis is a systematic examination of failed devices to determine the root cause of failure and to use such information to eventually improve component reliability [6]. Each failure, failure component, is unique and, therefore, should be treated as a single discrete failure. Failure analysis of capacitors should be augmented sufficiently to provide

significant recommendations to improve the component reliability. An effort should be made to assure all the aspects of the failure mechanism to be dealt with. As this theoretical approach is not easily attained, historical data concerning the basic failure mode should be studied thoroughly to reduce the number of steps necessary to determine the actual failure cause. Through effective root cause failure analysis, a great deal of data on HV ceramic capacitors, such as failure modes and failure mechanisms were obtained.

There are three types of typical failure modes for ceramic capacitors; open failure, electrical shorts or low resistance, and capacitance value being out-of-tolerance in terms of electricity. There are two HV ceramic capacitors failure regimes defined by the constructing materials: dielectric breakdown failure and adhesive failures (cohesive failure and adhesive failure).

One physical defect of key concern to HV ceramic capacitors manufacturers is delaminations. Delaminations, or separation of the epoxy and dielectric layers under cyclic thermal stress due to temperature fluctuations and in-circuit power on/off, are the root cause of failures during testing of components, low manufacturing yields, and the far more costly field failures. Delaminations are formed as the result of mechanical stresses created by the differences in the thermal expansion of ceramic-epoxy (C-E) interface during thermal cycle. Air discharge under voltage bias and subsequent arc tracking phenomenon can be accelerated by the presence of delaminations. Therefore, appropriate experiment is needed to estimate the reliability and understand the associated thermal fatigue failure phenomena for HV ceramic capacitors. The reliability of HV ceramic capacitors was assessed through accelerated lifetime testing (ALT). Thermal cycling (TC) test has the capability of ascribing the device failures to manufacturing process or material defects. Failed HV ceramic capacitor from this test was analyzed by root cause failure analysis to determine the main sources of failure. Also, flaws responsible for interfacial cracking were identified and process improvements were suggested to eliminate them. The B_{10} life of HV ceramic capacitors with failed data in ALT were subsequently compared with that of in the field. After satisfactory correlation between the experimental data and field data was observed, the acceleration factor (AF) was calculated by using power law relationship model [7]-[10].

We normally purchase and use the capacitors in good faith from approved vendors, but sometimes encounter catastrophic failures in incoming inspection or field and initiate corrective actions with the manufacturer afterward. This is because material properties and various geometric variables subject to manufacturing processes are random variables, which can cause uncertainty in product life. In addition, the method of qualification is not well established to recognize variations in material properties and manufacturing processes, either. In consequence, the capacitor users cannot provide meaningful feedback that could help the manufacturers detect and improve

their materials or the manufacturing process defects. It is known that dielectric breakdown is one of primary drawbacks for high dielectric materials, such as HV ceramic capacitor and multilayer ceramic capacitors [11]. Dielectric breakdown may occur as a result of excessive voltage applied to a dielectric, leading to rupture and an electrical short circuit. We can evaluate the failure rate for dielectric breakdown in terms of overstress failure, considering the probability distribution functions of the applied load and available strength. In this paper, a load-strength interference model [12]-[14], which is desirable as an alternative to testing potential options, was used to estimate the failure rate for dielectric breakdown due to partial discharge. But, this approach is based on the assumption that there is no degradation of the strength of a component with time. We must still fulfill the requirement of understanding the impact of variation because good data on load and strength properties are very often not available. The reliability estimate of HV ceramic capacitors was performed with statistics package (MINITAB Release 13).

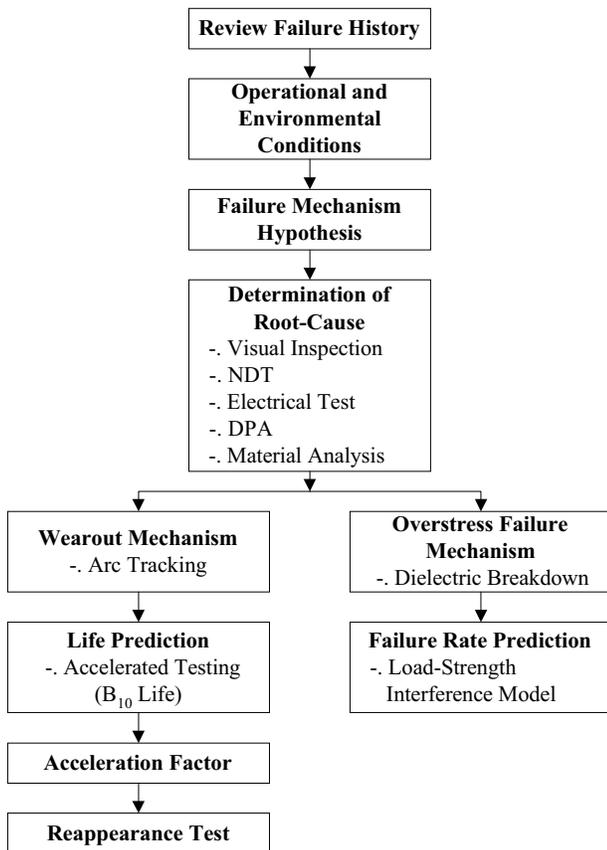


Figure 1. Flowchart of Failure Analysis.

II. Failure Analysis

A. Procedure of Failure Analysis

Failure analysis is designed to: identify the failure modes; identify the failure site; identify the failure mechanism; determine the root cause; and recommend failure prevention methods. The process begins with the most non-destructive techniques and then proceeds to the more destructive techniques, allowing the gathering of unique data from each technique throughout the process. This data when properly analyzed leads to a viable mechanism for the failure. The recommended sequence of procedures is: identification; failure history; visual inspection; electrical testing; non-destructive evaluation (NDE); destructive physical analysis (DPA) [15]. To increase the reliability, however, this information must be coupled with the results of failure mechanism modeling. The information provided by these physics-of-failure (PoF) models allows designers to select materials and package design attributes, which minimize the susceptibility of future designs to failure by the mechanisms identified in the degradation assessment [16]. Figure 1 shows the flowchart of failure analysis.

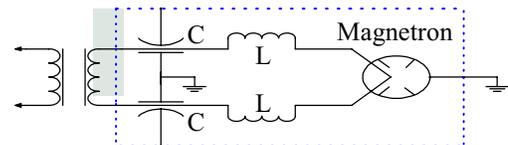


Figure 2. Equivalent circuit of magnetron for microwave oven (MWO).

B. Failure Analysis Results

The failed samples in this study were of Y5U-type HV ceramic capacitors, rated at 4000-volts DC (direct current) and nominal capacitance of 500pF, which obtained from the general population of field returns. The assembly construction is shown in Figure 2. A HV ceramic capacitor mounted on a magnetron for “LC” filters indicates short circuit under normal operating conditions in the field.



Figure 3. Photograph of 500pF 4000-volts Y5U HV ceramic capacitor, showing burnt material.

The level of inspection should be sufficient to assure identification of visual anomalies. Visual inspection revealed a surface damage to the capacitor outer case material as shown in Figure 3. The outer case was a PBT (Polybutyleneterephthalate) filled with epoxy resin (see Figure 4).

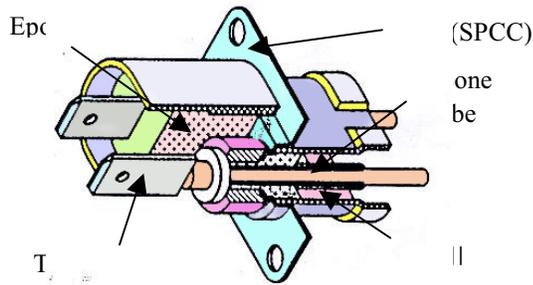


Figure 4. Construction of a HV ceramic capacitor.

Electrical parameters to identify which component is failed should be estimated during the non-destructive testing. Other parameters including capacitance (C), dissipation factor (DF or $\tan\delta$), and insulation resistance (IR) may be measured as required to assist the determination of the failure mode. C and DF were measured at 1 ± 0.5 -volts (rms), 1kHz. IR was also measured at 500-volts for 120 ± 5 -seconds. The failures were judged in accordance with the criteria of failure shown in Table I. The C, DF, and IR were excessive. Table I summarized these tests.

Table I . Failure criteria for test sample and test results

Failure Mode	Drift, Capacitance	Drift, $\tan\delta$	Drift, Insulation resistance	
Failed Sample	#1	82 μ F	398	Short
	#2	258 μ F	716	Short
	#3	176 μ F	655	Short
	#4	195 μ F	820	Short
	#5	977 μ F	1461	Short
Failure Criteria	More than $\pm 35\%$ drift from the initial value	More than 0.01 $\tan\delta$	Less than 10,000 mega ohm insulation resistance	

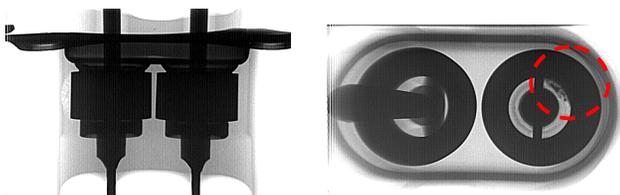


Figure 5. X-ray image of burnt component. Arrow at right indicates area where epoxy charred.

Non-destructive Evaluation (NDE) is designed to provide as much information on the failure site, failure mechanism, and root cause of failure without causing any damage to the product or obscuring or removing valuable information. X-ray is an effective inspection method to identify capacitor that has poorly

attached lead or inadequate encapsulation. However, the ceramic capacitor element itself is opaque to X-rays and therefore, internal element defects cannot be identified with X-ray. X-ray was performed and results are shown in Figure 5. X-ray analysis revealed a char at the C-E interface, which failed due to a delamination between the C-E interface.

Destructive physical analysis (DPA) provides a means for detailed analysis of the internal structure of HV ceramic capacitors. Full DPA was performed on components that failed in the field which revealed cracking of ceramic, chemical modification and evidence of increased conductivity of epoxy resin. Figure 6 shows cracks along the ceramic surface and combustion of epoxy resin by optical microscopy.

Table II . TGA results generated on cured epoxy resin

Contents	Epoxy I	Epoxy II
Decomposition Transition Temperature	257 $^{\circ}$ C	357 $^{\circ}$ C

Thermal analysis techniques are used to determine the glass transition and degree of cure as well as measuring mechanical properties such as expansion, contraction and modulus.

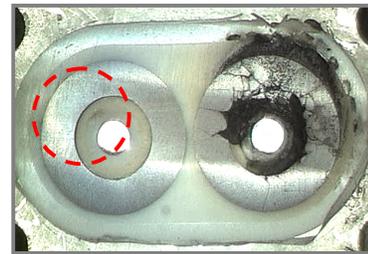


Figure 6. Optical photograph of a failed sample cross-section showing cracks along the ceramic surface and combustion of epoxy resin.

Thermogravimetric analysis (TGA) is a technique, which measures weight change in a material with increasing temperature. The information obtained can be used to evaluate thermal stability of materials and to provide material compositional analysis. Cured epoxy resin was analyzed over the temperature range ambient to 800-degrees centigrade using conventional TGA at 20-degrees centigrade per minute heating rate. All scans were run in flowing nitrogen atmosphere at 100-milliliter per minute. Approximately 10-milligram of sample was used. The TGA used was a TA Instruments SDT 2960 coupled to a Thermal Analyst 2100. Illustrated in Table II are the TGA results obtained when the cured epoxy resin is heated under standard conditions. The TGA results show that the cured epoxy resin undergoes thermal decomposition at 257 and 357-degrees centigrade for epoxy I and II, respectively.

Table III. TMA results for cured epoxy and ceramic

Contents		Epoxy I	Epoxy II	Ceramic
Glass Transition Temperature (T_g °C)		51	39	N.A.
CTE ($\mu\text{m}/\text{m}^\circ\text{C}$)	Before T_g	47	65	8~10
	After T_g	148	160	-

Thermomechanical analyzer (TMA) is generally used to measure the glass transition based on changes in coefficient of thermal expansion (CTE) which result as the free volume of the material changes at the glass transition. Shown in Table III is a TMA scan performed on a cured epoxy resin using TA Instruments TMA2940. The scan was run between -20 and 220-degrees centigrade at 10-degrees centigrade per minute in less than 40-minutes. It provides the glass transition temperature (T_g) at 51 and 39-degrees centigrade for epoxy I and II, respectively. Measurement of T_g by TMA is better for filled, highly crystalline, or cross-linked materials than measurement by DSC because the dimensional changes observed at T_g are usually fairly significant. The CTE prior to the T_g , one of the quality control parameters, is calculated for a particular temperature range from slope of the expansion curve using Equation 1.

$$\alpha(T_1 \text{ to } T_2) = \frac{[Y(T_2) - Y(T_1)] \times Y}{(T_2 - T_1) \times L} \quad (1)$$

where $\alpha(T_1 \text{ to } T_2)$ is the CTE for the temperature range T_1 to T_2 , $Y(T)$ is the Y -axis deflection at temperature, T is the temperature, Y is the Y -axis sensitivity, and L is the length of the sample respectively. Substituting the value from TMA data into Equation 1, we get the results of Table III. Dielectric and cured epoxy resin may exhibit large anisotropy in the CTE, producing significant thermomechanical stresses in C-E interface. As described in Table III, The CTE of ceramic, is approximately 8 $\mu\text{m}/\text{m}^\circ\text{C}$, where as the CTE of epoxy resin is approximately 138 $\mu\text{m}/\text{m}^\circ\text{C}$. This can cause the interfacial cracking of C-E interface under normal operating conditions because of CTE mismatch.

Table IV. Porosity and density results

Absolute density	5.25 g/cc
Open porosity	0.22 %

The differential scanning calorimeter (DSC) is used for analyzing a material's glass transition, degree of cure and cure state. Residual cure in the material is determined by calculating enthalpy of the exothermic reaction. DSC also has been extensively used to study the cure reactions of epoxy resin systems [17]. The T_g measurements for cured epoxy resin carried out by DSC using TA Instruments DSC 2010. Sample of

about 5-milligram were measured under a nitrogen atmosphere from ambient temperature to about 160-degrees centigrade at a rate of 10-degrees centigrade per minutes. The sample tested is epoxy resin, which makes diglycidyl ether of bisphenol A (DGEBA) prepolymer cured with acid anhydride at 100-degrees centigrade for 5-hours. The results of T_g are shown in Figure 7 and 8 for the epoxy I and II. We found that the T_g shifts appears to the same materials. This fact would be due to the differences of degree of cure. The shift of T_g in various samples for epoxy I and II suggests that epoxide group in DGEBA after curing reaction having intact prepolymer molecules and monoglycidyl ether of bisphenol A because of incompletely cured epoxy resins. As is shown in Figure 7, an exothermic peak due to the postcure of unreacted functional groups began just at the temperature of isothermal cure. The existence of a peak in rate curve of isothermal cure suggests that the third-order kinetics being predominant in the curing reaction of DGEBA with acid anhydride.

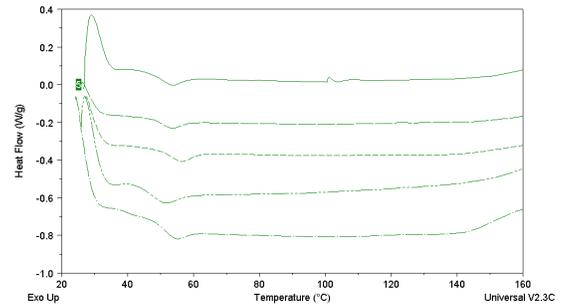


Figure 7. DSC curves for isothermal cure of DGEBA with acid anhydride for epoxy I.

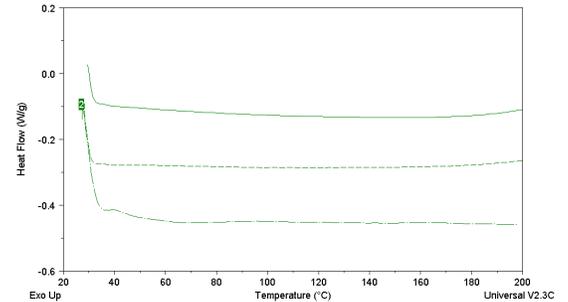


Figure 8. DSC curves for isothermal cure of DGEBA with acid anhydride for epoxy II.

In the case of HV ceramic capacitor, open porosity and pore size distribution are one of the factors in adhesive failure mode because adhesion depends on surface contact and surface condition. This is because adhesive force is enhanced with corresponding ceramic surface conditions. Table IV shows the open porosity and absolute density using Archimedes method. As these results show, compared with other electronic barium titanate BaTiO_3 (called later BaTiO_3) matrix, this value is somewhat lower. We investigated micro-morphology of non-adapted specimen using scanning electron microscopy (SEM).

We did some pretreatment for investigation. We decapped specimen using knife and did gold coating for electric conductivity. The SEM photograph of morphology of ceramic outer/inner surface is shown in Figure 9 and 10. Ellipse shapes surround the open pores the size of which range from 2 to 5 microns. These offered interface delamination points and interface crack initiation at these locations firstly could be expected. Adhesive forces at the C-E interface might be weakened as a result of the repetitive stress experienced during normal operation conditions. Interfacial crack at this site propagated along weakened C-E interface of HV ceramic capacitor. Large open porosity and pore size distribution of C-E interface both can be contributed to the initiation of adhesive failure.

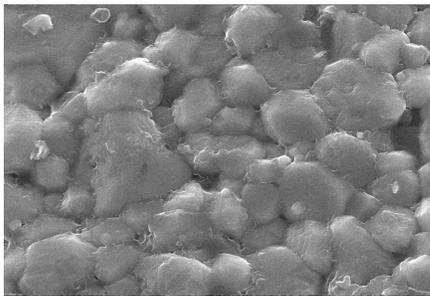


Figure 9. SEM photograph of morphology of ceramic outer surface. (2500X)

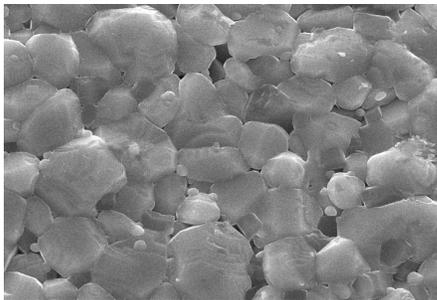


Figure 10. SEM photograph of morphology of ceramic inner surface. (2500X)

III. Failure Mechanisms and PoF Models

The failure modes observed in the tests were increase in $\tan\delta$, C, degradation of IR, and short-circuiting. The failure mechanisms obtained by the failure analysis were summarized in to the categories of arc tracking (or combustion) due to delamination as a wear out failure and dielectric breakdown as an overstress failure.

A. Analysis of Arc Tracking (or combustion)

The rate and degree of curing depends on time and temperature, as well as on catalyst amounts. If adhesives experienced cyclic fatigue loads due to the CTE mismatch between the C-E interface, it is accompanied by a volume contraction of the material at a later stage of conversion of monomer to polymer, which will cause shrinkage stresses or

thermal residual stresses at C-E interface to induce the delamination and interfacial breakdown in worst case. Also the morphology and roughness of ceramic surface under operating condition will be affects the bonding force. An arc tracking due to delamination was observed in withstanding voltage test after TC test. In this type of failure, $\tan\delta$ and C were in tolerance but the IR was excessive, which was followed by the degradation of IR by leakage on the C-E interface. This resulted in short-circuiting by arc tracking on the C-E interface.

B. Physics of Arc Tracking

Start and extend of arc tracking depends on the type of insulation material and construction, the power and frequency, and environmental factors, such as temperature, pressure, and humidity. Arc tracking [18] results from the formation of a conducting path in physical defects such as delamination or cracks on the C-E interface, and can often be observed on the interface where there is a maximum exposure to the foreign materials such as moisture, dust, active ions, and so on. The conducting paths can also be accelerated by conversion of carbonized epoxy to graphitic of epoxy composition. Once scintillation (or random momentary breakdown) initiated, the electrical arc propagates along the C-E interface and to the adjacent epoxy resin, causing a permanently shorting. As a result of heating due to a high current between the C-E interface has become conductive and even after ceramic was destroyed (probably because of scintillation) excessive current was drawn through the epoxy resin. Arc tracking phenomenon can be observed by visual inspection as “ track” on the failure site as shown in Figure 11.

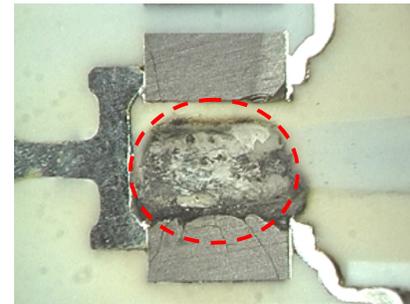


Figure 11. Optical photomicrograph showing a sample failure due to arc tracking.

C. PoF Modeling for Arc Tracking to Estimate of Time to Failure

Mechanical stresses in electronic assemblies result from the thermal and stiffness mismatch of bonded materials. One of the most significant problems encountered with HV ceramic capacitor has been the formation of interfacial delamination during service operations due to TC. A significant temperature cycling is present in C-E interface, and free-edges of the bonding interfaces in such structures suffer high stress gradients, which eventually cause cracking of the interfacial delamination [19]. ALT of HV ceramic capacitor is needed to insure the reliability

of these devices. For the evaluation of product life by wear out failure mechanism, it consists of two steps: calculating AF relating the failure distribution under ALT conditions to the failure distribution under actual use conditions. These AF are determined using PoF models for the failure mechanisms identified in the degradation analysis; and determining failure distribution for the capacitors under ALT test conditions consisting of appropriate loads and levels to produce maximum test time compression without shifting the dominant failure mechanisms [20].

TC fatigue failures can be expressed with a simple power law relationship, i.e:

$$\Delta\sigma(N_f)^b = C \quad (2)$$

where $\Delta\sigma$ is the strain or stress range, N_f is the number of cycles to failure, b and C material constants. Recognizing that the thermal stresses and strains are directly proportional to the temperature cycle range, the fatigue power law relationship can be rewritten in terms of the temperature change, ΔT , as

$$\Delta T(N_f)^b = C \quad (3)$$

where ΔT represents the magnitude of a temperature change. The AF relating the time compression of the test to use conditions is calculated by

$$AF = \frac{N_{f(field)}}{N_{f(test)}} = \left(\frac{\Delta T_{test}}{\Delta T_{field}} \right)^{\frac{1}{b}} \quad (4)$$

assuming that the material fatigue exponent b does not change between the test and the use temperature conditions. Life data can best be described by the cumulative Weibull distribution for a given cyclic condition.

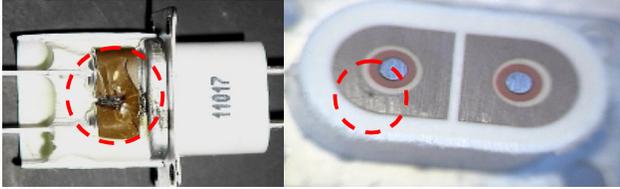


Figure 12. Optical photomicrograph of an overstress site in a ceramic capacitor, resulting in localized dielectric breakdown. Fracture surface of a sample failed after withstanding voltage test. Failure analysis on these sample revealed that the voids are the main source of failure.

D. Analysis of Dielectric Breakdown

HV ceramic capacitors in this application are used as suppressors to prevent high voltage transients from damaging peripheral components, or as filters to prevent the transmission of noise or RF (radio frequency) energy to the circuit. However, exceeding the dielectric breakdown voltage of the ceramic may produce internal fracturing that will cause immediate shorting or

latent leakage paths, depending on the energy of the transient. Dielectric breakdown failure due to partial discharge of the dielectric was observed in the withstanding voltage test. In this type of failure, the weak points were the voids (or pores) and cracks contained in the ceramic, and the discharge of those weak point seem to be the main source of electric breakdown. These indicated that the partial discharge of cracks and voids were the root cause of dielectric breakdown in ceramic.

E. Physics of Dielectric Breakdown Failure

There will inevitably exist defects of voids (or pores) and slight cracks in the ceramic due to the limit of manufacturing technique. There may be several intrinsic factors affecting breakdown strength of BaTiO₃, such as porosity, grain boundaries, and domain wall instability [21],[22]. But, in general, the dielectric breakdown in insulating ceramics has been believed to be caused by partial discharge within pores in the materials [23]. These pores are usually filled with gas (air) of lower breakdown strength than BaTiO₃ matrix. Moreover, the permittivity of the air is much lower than that of the BaTiO₃, which causes the field intensity in the pores to be much higher than in BaTiO₃ matrix. Because of the high dielectric constant of BaTiO₃ in high electric field, electric field inside pores in BaTiO₃ ceramics must be intensified much more than in other insulating ceramics. Accordingly, under working stress of the ceramic capacitor the voltage across the pore may exceed the gas breakdown value and may initiate partial discharge in the pore according to Paschen's curve [24]. Partial discharge in certain of these pores may result in transient over-stressing of other series pores and therefore cause them to discharge [25]. If this phenomenon is accelerated under high voltage condition, excess energy accumulates at a particular region. Finally the stored energy abruptly dissipates as destructive energy. These discharges can cause local heating or over-stressing of the remaining ceramic dielectric, so lead to avalanche breakdown. This phenomenon is called dielectric breakdown. Figure 12 shows the fracture surface of a sample where the source of the failure is a void in the bulk ceramic.

Failure of this type was seldom observed in the HV ceramic capacitors. Since the energy stored at a particular region is small enough to be dissipated under normal service condition, the probability of such failures in service is extremely small.

F. PoF Modeling for Dielectric Breakdown to Estimate of Failure Rate

We must design the strength of components to assure that we meet the load conditions for a reasonable level of risk. The load-strength interference approach to modeling the reliability of a component, based upon knowledge of load and strength probability distribution functions, is developed and applied to design of components. Note that we are considering situations where the mean strength remains constant, i.e. there is no strength degradation with time.

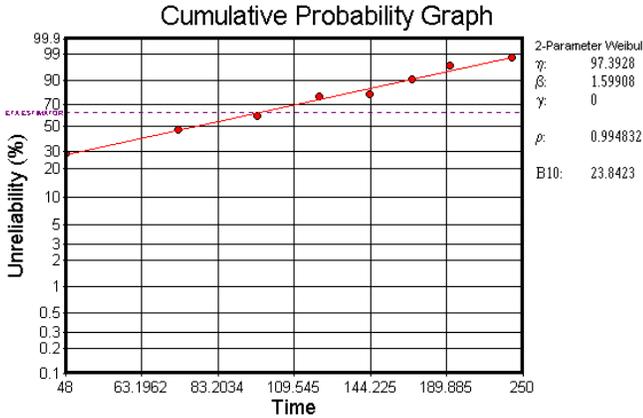


Figure 13. Thermal cycling life distribution of HV ceramic capacitor resulting from TC test.

For most products neither load nor strength are fixed, but are distributed statistically. If an event occurs in which the two distributions overlap, i.e. an item at the extreme weak end of the strength distribution is subjected to a load at the extreme high end of the load distribution, such that the "tails" of the distribution overlap, failure will occur. The safety margins is the relative separation of the mean values of load and strength and the loading roughness is the standard deviation of the load; both are relative to the combined standard deviation of the load and strength distributions. If we consider normally distributed strength and load, the reliability of a part, for a discrete load application, is the probability that the strength exceeds the load:

$$R = \Phi \left[\frac{\bar{S} - \bar{L}}{(\sigma_S^2 + \sigma_L^2)^{1/2}} \right] \quad (5)$$

$$= \Phi(SM)$$

where \bar{S} is the mean of strength, \bar{L} is the mean of load, σ_S is the standard deviation of strength, and σ_L is the standard deviation of load, respectively. The reliability can also be determined by finding the value of the standard cumulative normal variable from the normal distribution tables.

IV. Estimation of Reliability

As explained in Section III, the failures of HV ceramic capacitors are generally classified into two types; arc tracking and dielectric breakdown failure. Those two types seem to occur independently of each other.

A. Estimation of Time to Failure from Arc Tracking

1) *Experimental Work*: Temperature cycling occurs due to a TC environment or due to device power cycling. Under these conditions, sufficiently large tensile and shear stresses can arise in the C-E interface to cause interfacial cracking. The experimental work basically consisted of determining the arc tracking time to failure of HV ceramic capacitor before and after TC test. This would establish if a short TC test would screen out

all arc tracking. The capacitors used in the ALT were of Y5U-type HV ceramic capacitors, rated at 4000-volts DC and nominal capacitance of 500pF from standard production batches. The capacitors were characterized by measuring the C, DF at 1kHz, and IR before the test. No significant electrical differences were found. Thirty HV ceramic capacitors were used for TC test. These capacitors were subjected to TC test. Temperature limits for this condition are -40 and +120-degrees centigrade and the 300 cycles consist of a one half hour dwell at each extreme, with five minutes maximum transfer time. The capacitors were not powered or connected electrically during testing. Withstanding voltage test was performed after every 24 cycles are completed. Devices were considered failures if dielectric breakdown occurs under withstanding voltage test. The C and DF were in tolerance but the IR was excessive. Capacitors that fail the TC test undergo failure analysis. The process of failure analysis provides confirmation of the dominant mechanism and the failure site. This is critical to ensuring that testing is representative of "field conditions" or anticipated environment. Selective capacitors failed in the TC test were mounted in epoxy and polished, with the final polish using 0.1- μ m alumina powder. These samples were examined using both optical and electron microscopies. The cross section surface is examined at approximately five mil intervals for interfacial cracks. Figure 13 shows the cumulative Weibull distribution of HV ceramic capacitors.

2) *Results and Discussion* : Failure analysis showed an interfacial cracking failure due to delamination as shown in Figure 14. This results are very similar to those obtained from field failed samples, and indicate the same trend in terms of failure mechanism. For HV ceramic capacitor, the Weibull parameters were determined by fitting to a test data, and can be expressed as

$$F(t) = 1 - \exp \left[- \left(\frac{t}{97} \right)^{1.599} \right] \quad (6)$$

where t is the random variable, the shape parameter of Weibull slope is 1.599 and the characteristic life at 63.2-percent is 97 cycles. And B_{10} life is 23 cycles. Note that B_{50} life is meaningless to consumers.

Failed data in the field were gathered over a period of one year to predict the lifetime. Here, the life distribution of HV ceramic capacitor is modeled as expressed in (7),

$$F(t) = 1 - \exp \left[- \left(\frac{t}{2028} \right)^{1.557} \right] \quad (7)$$

where t is the random variable, the Weibull slope is 1.557 and the characteristic life at 63.2-percent is 2028 cycles. And B_{10} life is 478 cycles. This is plotted the field cumulative failure data which is gathered for one year. The equation (7) was obtained from Figure 15. It can be seen that there is a good correlation between the field life data and the experimental life data due to the almost same in the shape parameter of the distributions.

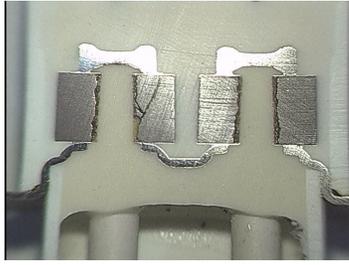


Figure 14. Optical photomicrograph showing a sample failure due to arc tracking. Failure analysis on these sample revealed that the dematinations are the main source of failure.

We can apply the AF to data accumulated in test to assess the relationship between the test life and field life. We can say the relationship between test time and field life can be expressed for a given failure mechanism as:

$$AF = \frac{t_{f(field)}}{t_{f(test)}} = \frac{B_{10(field)}}{B_{10(test)}} = \frac{478}{23} \approx 21 \quad (8)$$

We then apply Equation (8) to Equation (4) to calculate the value for the AF exponent, $1/b$. ΔT_{test} is the difference between the temperature cycling limits, or 160-degrees centigrade. Assuming ΔT_{field} is conservatively 50-degrees centigrade, values for the AF exponent, $1/b$, when using the value of 21 for the AF, is approximately equal to 2.6.

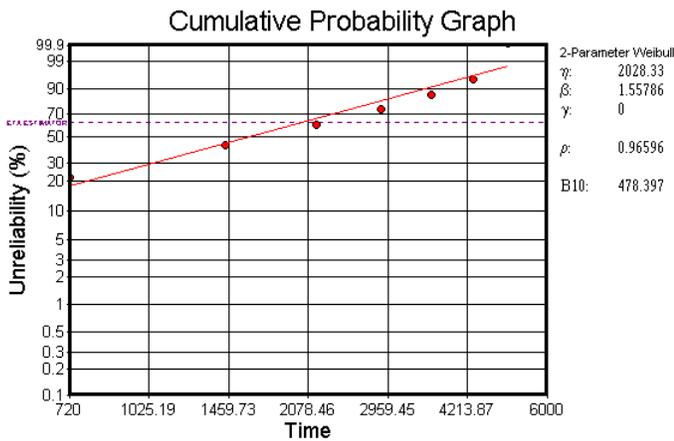
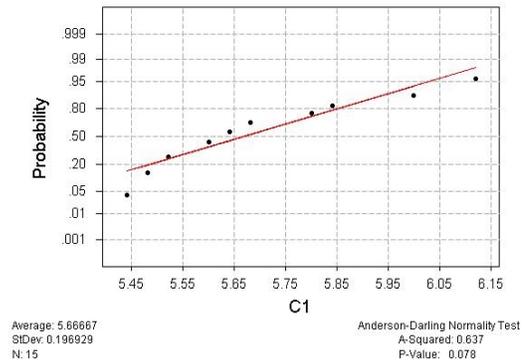


Figure 15. Field cumulative failure distribution of HV ceramic capacitor.

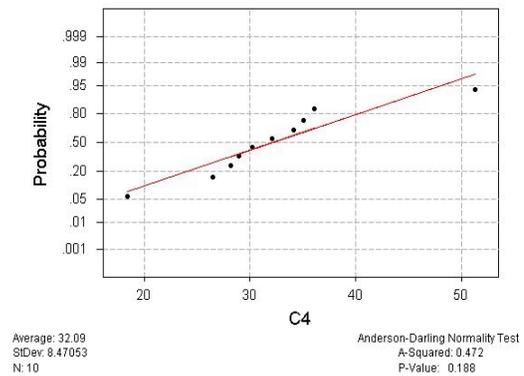
Assuming that the number of on-off cycles for operating time of microwave oven (MWO) is thirty minutes per day every day of the year and if no failures were observed during 300 hours test period, a minimum lifetime equates to a period of approximately 34 years with respect to temperature cycling induced failure for HV ceramic capacitor.

B. Estimation of Failure Rate from Dielectric Breakdown

1) *Experimental Work:* We can estimate of failure rate for HV ceramic capacitor, explicitly considering the probability distribution functions of the applied load and available strength with a load-strength interference model. The normal rated voltage for capacitor is 4000-volts DC and the design load 4000-volts. A primary concern is electrical overstress failure. We samples 10 devices from manufacturer and measures the breakdown voltage, V_B . We find by plotting using statistics package, that the breakdown voltage is normally distributed. In order to evaluate the reliability, however, we must know the loading roughness. We measure the voltage across the capacitor under operating conditions, and then find by plotting, that the load is normally distributed with a mean of 32000-volts.



(a) Load distribution (n=10).



(b) Strength distribution (n=10).

Figure 16. Normal probability plot for measured load and strength of capacitor.

2) *Results and Discussion:* The results are shown in Figure 16 and Table V. We make the following calculation using our simple load-strength interference model in Equation (5). The estimated failure rate at 95-percent confidence level under the normal operating is shown in Table VI and VII. The result of Table VI shows a situation where loading roughness is low, but due to a large standard deviation of the strength distribution the

safety margin is low. We may interpret the results to show that this device may be expected to experience failure, due to the HV ceramic capacitor, on the application of the first load. Extreme load events will cause failure of weak items. However, only a small proportion of items will fail when subjected to extreme loads. This is typical of a situation where quality control methods cannot conveniently reduce the standard deviation of the strength distribution (e.g. in electronic device manufacture, where 100-percent visual and mechanical inspection is not always feasible).

Table V. Normality test results

Manufacturer	Strength	Load	Remarks
A	0.188	0.078	P Value More than 0.005

Table VI. Estimated mean and variance for a HV ceramic capacitor

Distribution	Strength	Load
Number	n = 10	n = 10
Mean(X)	32.09	5.66
Variance(S ²)	71.74	0.038
Mean of population(μ)	26.5 $\leq \mu \leq$ 38.5 (Student t distribution)	5.5 $\leq \mu \leq$ 5.8 (Student t distribution)
Variance of population(σ^2)	33.9 $\leq \sigma^2 \leq$ 239 (Chi-square distribution)	0.018 $\leq \sigma^2 \leq$ 0.12 (Chi-square distribution)

Table VII. Estimated reliability for a HV ceramic capacitor

Manufacturing	A
SM(Safety Margin)	3.12
R(Reliability)	0.99902
Failure Rate	0.098 %

Conclusions

It was confirmed that the failure modes of HV ceramic capacitors are evidenced by increases in DF, degradation of IR, and short-circuiting through the root cause failure analysis. The failure mechanism leading to these modes is arc tracking. This failure mechanism, which is related to material, structure, and the manufacturing process of HV ceramic capacitor has more effect on reliability under actual service conditions.

A power law model was used to study the time to failure of arc tracking in HV ceramic capacitors subjected to TC test. The results of modeling analysis suggest that a thermal gradient significantly affects C-E interface delamination. This is because the mechanical stress occurs considerably during TC period. The Weibull parameters for arc tracking of HV ceramic capacitor were determined based on the result of experiment. After

satisfactory correlation between the experiment and field was observed, the calculation of AF on the adhesive failure life of C-E interface in HV ceramic capacitor was determined experimentally. Arc tracking can be described by the cumulative Weibull distributions with shape parameter $\beta=1.5$.

A load-strength interference model has been described for design validation of HV ceramic capacitor and its capability to replace the conventional approach methods such as safety factor and derating rule to verify the design. A load-strength interference model can be used to estimate the failure rate for overstress failure mechanism. In this study, dielectric breakdown failure can be described by normal distributions.

Fracture mechanics approaches can be used to study reliability problems such as a adhesion related failure in electronic devices. The J-integral criterion is mostly used to characterize both polymeric materials and interfacial adhesion. Further study based on fracture mechanics approach using PoF model is left as the future research area.

Acknowledgments

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Thermal and Moisture Induced Stressing Effects of RF Power Amplifier Modules

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Abstract

The trends in RF Power Amplifier(RFPA) Module for handset is optimizing active device technology, circuit topology and packaging to enhance cost, size, performance, ease of implementation. For the package in RFPA Module manufacturing, device-to-board attach solder reflow condition and moisture sensitivity level(MSL) are the most challenging area for further improvement in thermal management due to "Lead-Free" application which causes catastrophic failure by high temperature application. In consequence, there have been faced with industrial requirements to improve both MSL and reflow temperature without any catastrophic phenomena such as Solder Extrusion and Solder Flow in RFPA Module. This paper discusses various considerations to define critical factors that will effect on thermal and moisture induced stress in RFPA Module in long term reliability assurance at the package design stage. On the analysis of severe failure mechanisms in RFPA Module, identified the cross effects on various characteristics of moisture induced package failures causing from alloy composition of components termination, behaviors of component attachment materials for active/passive, and substrate metallization with its own material. Also, best raw material combinations and critical consideration factors for package integrity of RFPA Module with MSL reliability are discussed.

I. INTRODUCTION

Power amplifiers are used in the final stage of wireless transmitters to increase the rated power level(Fig.1). Power amplifier modules lend themselves extremely well to phone design because they have all matching circuitry and all or most biasing circuitry included in the module. The module substrate can be FR-4 PCB material (similar to the phone PCB) or a higher dielectric material to reduce the physical size of distributed matching elements. The packaged semiconductors gave way to discrete semiconductors die mounted directly to the substrate material and wire bond connected to the circuit. An epoxy material is applied over the top of the die to encapsulate them and provide a measure of humidity resistance[1].

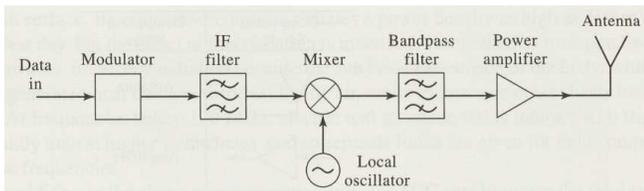


Fig.1 Block diagram of a basic radio system - transmitter

RF PA modules provide a particular function as a fully integrated component, which includes both active and passive components such as Si/GaAs die, Register, Inductor and Capacitor(Fig.2). The passive elements are implemented either as integrated passives in the die, or are mounted onto the module's substrate. The active components are mounted onto the module's substrate as packaged and wire bonded. Radio on a single chip is not technically feasible. As a result, multi-chip modules, which integrate different type of chips inside a single mechanical housing, become an attractive alternative[2].

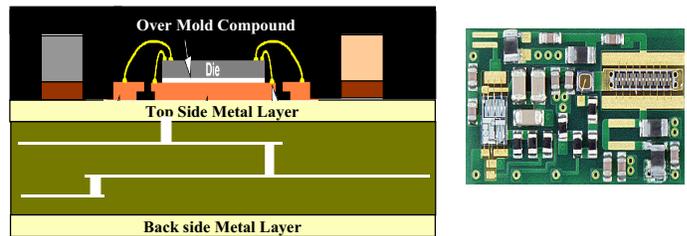


Fig.2 Cross sectional (Left) and top (Right ; before encapsulation) view of RFPA Module

Moisture inside RFPA Module turns to vapor and tries to expand when the Module is exposed to rapid high temperatures during reflow soldering. The internal vapor pressure can cause separation of the Module from the semiconductor chip or printed circuit board, and damage to thin films and wire bonds. In RFPA modules, the component attach solder was extruded under the components or flowed on the PCB top surface/metal runner due to over temperature and excessive moisture in the module. RFPA modules that are a Leadless Chip Carrier if not handled properly, can cause severe damage during the solder reflow attachment process to printed circuit boards (PCBs). The damage occurs as a result of Solder Extrusion, Solder Flow/creeping and / or delamination between internal package interfaces (i.e., die surface/PCB metal runner and encapsulant material). In this Module, the Solder Extrusion and Solder Flow/creeping were major contributors to the package reliability problem that causes open/short failure of the Module's circuitry(Fig.3).

To reduce the Solder Extrusion and Solder Flow failure, various consideration and evaluation were performed such as PCB material, PCB top metal plating scheme, solder alloy/volume and made an improvement on package reliability and MSL level.

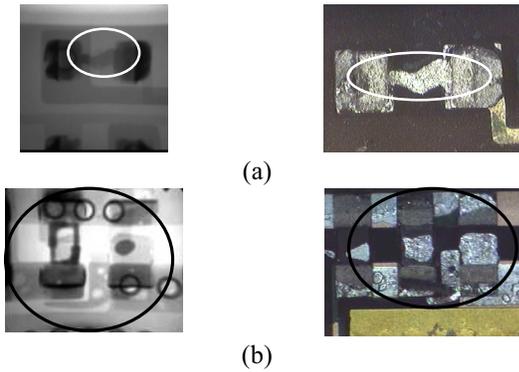


Fig.3 Solder Extrusion / Flow failures

(a) Typical solder Extrusion under the passive component; Left : X-ray photo, Right : Microscope image after mechanical decapsulation, (b) Typical Solder Flow; Left : X-ray photo, Right : Microscope image (Extrusion/Flow)

II. RELIABILITY GOALS AND APPROACH

Currently, RFPA module's moisture sensitivity level in ASE Korea is MSL3 at 225°C reflow temperature compare to MSL4 with competitors. To improve moisture sensitivity level and reduce the catastrophic phenomena, i.e., Solder Extrusion, Solder Flow, various considerations for the different raw material selections and process treatments were conducted to enhance moisture sensitivity level, currently from MSL3 to MSL2.

The Solder Extrusion and/or Solder Flow failure could be caused not only by humidity/temperature but also material properties such as diffusion mechanism of solder alloy. One of the most important root cause of this type of failures is the rapid heating of the moisture absorbed within the plastic encapsulant and Printed Circuit Board. Any absorbed moisture is quickly turned into heated steam. A number of factors can influence on the moisture sensitivity of RFPA Module. These include both the internal dimensions and design of the PCB, the external dimension of the package and the physical properties of the die attach material and mold compound. Also, the die dimensions can affect moisture sensitivity. The most important two factors, which can influence on the moisture sensitivity of RFPA Module, are the amount of absorbed moisture and the solder reflow temperature profile.

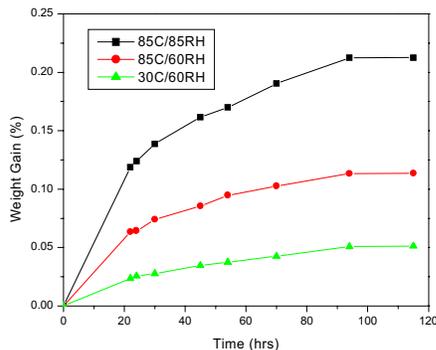
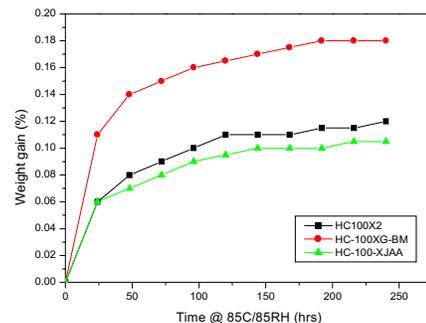


Fig.4 Moisture absorption rate(%) – RFPA Module

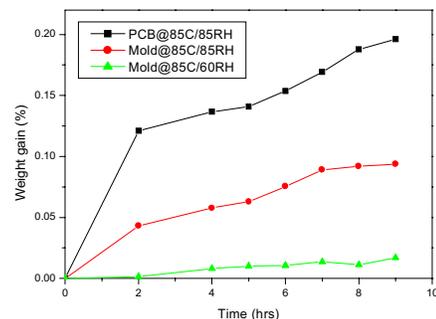
These two factors can fatally induce reliability failures such as Solder Extrusion and/or Solder Flow, that are caused by 1) Physical properties of the printed circuit boards 2) Physical properties of the mold compound 3) Reflow Temperature 4) Relative humidity of the ambient atmosphere 5) Time duration at those conditions 6) Component attach solder and its termination.

The absorption rate (Weight %) of moisture into the mold compound and PCB is temperature and RH (Relative Humidity) dependent[3]. The higher the temperature, the faster the surrounding moisture will penetrate to the mold compound and PCB. The absorption process will be continued until the internal moisture concentration reaches equilibrium with the ambient relative humidity. Thus the higher the relative humidity, the greater the amount of absorbed moisture within the package. Figure 4 indicates moisture absorption rate (weight %) varying from different moisture soak requirements. In the most case, soak time within 20hrs, has steepest moisture absorption trend. Molding compound samples, which have different 3 types base material properties from supplier, evaluated to measure the amount of moisture soak with time varying under 85C/85RH. HC100X2, mold compound currently used for RFPA Module, has reached to 0.1% weight gain as shown in Figure 5.

To identify sensitive core materials in the moisture, mold encapsulant and bare PCB are measured those weight gain (weight %) with the same method as before. PCB reaches at about 0.2 % of the moisture after 9 hours at 85C/85RH condition. From these results, recognized that PCB could have 2 times much more the moisture absorption than mold compound encapsulant does under the 85C/85RH as shown in Figure 5.



(a) Mold Compound



(b) PCB Vs Mold Encapsulant

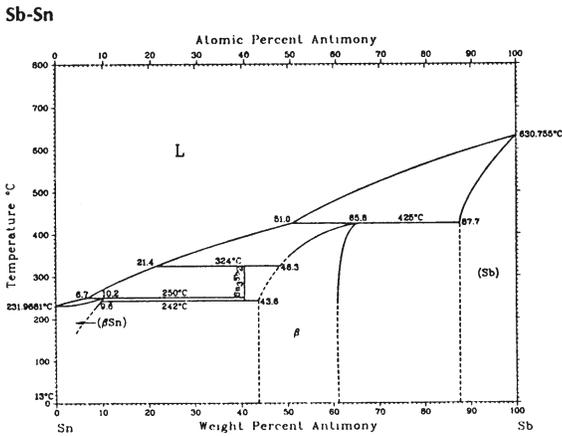
Fig.5 Moisture absorption rate (Weight %)

From the standpoint of moisture absorption, the nature of PCB itself is more key contributor than mold compound and acceleration MSL3 testing is not a correct method for RFPA modules. Therefore, we did not apply the accelerated MSL condition through RFPA module experiment. Accelerated soak times may vary due to material properties, i.e., encapsulant, PCB, etc[3].

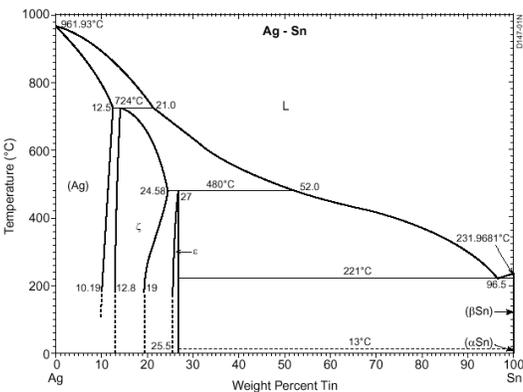
RFPA module, which has a leadless type backmetal for the package, is directly heated and this direct heating is at the heart of the problems. Earlier package groups were concerned with the heating of the leads only. Some degree of heating was present in the body due to the thermal conductivity of the lead frame, but this did not produce the same level of thermal stress that devices are now subject to RFPA modules. The heat from soldering causes a buildup of additional stresses within the device that were not present from the manufacturing process. Reflow process is well-known area where temperatures can reach levels sufficient to cause of the package integrity problems. When a package is heated, the thermal stresses in the device are applied to the active and/or passive components and causes severe problems such as short/open circuitry.

exposure, also affect the package integrity of RFPA module. In general, the slower the ramp rate and the lower the maximum temperature, the less the probability of potential damage due to moisture sensitivity. The type of equipment used influences the dynamics of the reflow process. To avoid thermal shock of the RFPA module the maximum heating and cooling rates (i.e., ramp rate) should be controlled. The amount of thermal energy absorbed varies with locations. Therefore, the surface and bottom temperature of the device is not uniform. If not properly planned, component overheating is possible and causes unwanted Solder Extrusion and Solder Flow failure.

Generally, Sn95%Sb5% high temperature solders which we use in normal production has its solidus, 235degC and liquidus, 240°C as illustrated in the phase diagram in Fig6. This phase diagrams can provide the melting temperatures of the “virgin” filler metal and of the abutting components[4]. Since this melting characteristics are a little different by reference book, it’s melting characteristics are very complicated to understand when is it melt or not in the possible meting temperature. So, it is need to verify which one (Tin-antimony and Tin-silver) is appropriate for RFPA module at the actual environment and it is true that the amount of moisture inside of package is critical factor to accelerate solder meting by diffusion of the moisture inside the package. To see solder meting trend at the known temperature range for both Sn95%Sb5% and Sn95%Ag5%, evaluation was performed with MSL3 conditions at the different temperatures (Table 1). And, it is confirmed that the tin-antimony(Sn/Sb) solder is the right solution for RFPA modules.



(a) Antimony-tin phase diagram



(b) Silver-tin phase diagram

Fig.6 Phase Diagram of Sn/Sb, Sn/Ag solder[4]

However, the profile of the solder reflow process, which includes preheat, ramp up and maximum temperature

Table1. Solder Melting Behavior with 230/240/250°C Peak Temperature in Reflow Profiles

Solder	230°C	240°C	250°C
Sn95%/Ag5%	None	Melting	Flowing
Sn95%/Sb5%	None	Melting/Flowing	Flowing

Also, the passive component’s termination material (AgNiSnPb, AgNiSnSb, etc.) is one of the causes of Solder Extrusion/Flow failure in RFPA module. Therefore, the termination material (solders) should be controlled with high temperature solder (SnSb) if possible.

III. EVALUATIONS

The major responses of below were all the failure modes found from MSL test, Delamination between layers, Solder Extrusion, Solder Flow, etc., after experiencing proper level of preconditioning. The main purpose of the evaluations were to determine and select the combination of most reliable performance in terms of MSL

A. LAMINATE MATERIAL

As early mentioned, the most difficult question regards the choice of the RFPA Module’s printed circuit board. Thereby, various vendors’ PCB was selected for moisture sensitivity level evaluation such as; supplier A, B, C, D etc. However, supplier A, B, C were the laminate materials in our concern. From our bench marking studies, we found several RFPA

modules, which has supplier A as its substrate, and supplier B/C is the ones we had applied in our RFPA modules(Table2).

Table2. The properties of the laminates

Laminates	Er	Tg	H2O Absorption
Supplier A	3.9 to 4.6	180°C	0.20%
Supplier B	3.5 to 4.3	180°C	0.12%
Supplier C	4.3 to 4.5	180°C	?

Er : Relative Permittivity, also called Dielectric Constant

Tg : Glass Transition Temperature

The PCB of supplier B shows a best performance from the point of thermal and moisture induced stress effects. Fig. 7 shows the result of the heat block experiment after 6 hours of moisture soak at 85°C-85RH. Though we can not say the difference exactly for the supplier B and C, supplier A is clearly showed the worst and supplier B reveals the best performance in the interested temperature range (230 ~ 250°C). In repeated experiment, we also confirmed this fact, but were still in difficulty to say the superiority between the rest two.

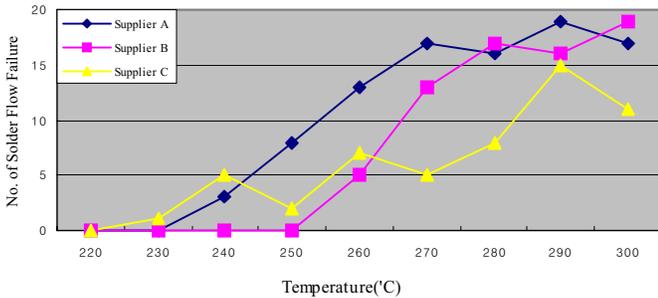


Fig.7 The heater block experiment reveals best performance on supplier B in the interesting temperature range (230 ~ 240°C)

B. PCB TOP METAL PLATING SCHEME

It has become clear that *'thickness'* is the most influential characteristic of the Au deposit as it relates to the ultimate integrity of the solder connections. Thinner, less porous Au deposits are extremely important for several reasons ; 1) Adequate solderability protection at a lower cost, 2) Lower probability of solder connection embrittlement, 3) Reduced voiding in solder connections, 4) Reduced localized Sn depletion[5].

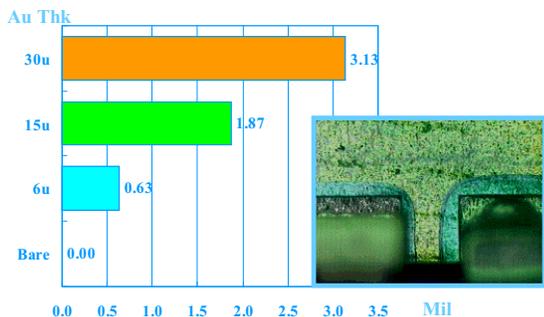


Fig.8 Solder creeping distance by Gold plated thickness after reflow

In experiment build, the full-bodied PCB group showed the severe solder creeping under the solder mask as seen in Fig.8. Actually, the thinner gold metallization of PCB reveals the best performance from the point of solder flow and/or extrusion. Also, the heater block experiment reveals best performance on supplier B material compare to supplier C.

Below 0.5% of gold in the solder no difficulties in soldering are encountered, but at a higher concentration the solder becomes slowing-moving (sluggish) during cooling on account of the primary crystallisation of gold-tin plates[6].

C. SOLDER ALLOY

The antimony content of the solders is a matter of unceasing debate. Some standards require a maximum content of antimony, whereas others require a minimum content. The soldering properties of solders are not sensitive to small amounts of antimony. A small amount of antimony in the solder may be of advantage, as it promotes the elimination of aluminium contamination by the forming of solid AlSb intermetallic, which is taken up in the dross. A silver concentration below 2% does not cause any deterioration in soldering results, but at a higher silver content grittiness of the surface due to the intermetallics that are formed can be observed[5].

While we have used 95Sn5Sb for all our PA modules, other company's standard was 96.5Sn3.5Ag, the eutectic composed solder. Even though the moisture makes various types of failure mechanisms, most of the actual failure is made by the solder flow above its melting point. In this point of view, the solder we have applied for our PA module has great advantage near the customer's reflow temperature region.

D. SOLDER QUANTITY

As previously mentioned, the MSL response is quite sensitive to the flow of molten solder and moisture. This time, we worked the quantitative approach, which can make sufficient soldering but least flow when it is molten. We made two type of solder screen print stencil of different aperture sizes. Area covered by solder paste after printing – rated toward the component land size. We have used 4mil thick stencil for all our PA modules. This thickness is in the thinner range that applied in SMD, but compare to the thicker one, thinner stencil has advantages in terms of covering area. It means that it has more room for component placement position variation. Even the component is placed off the target, the holding flux and solders pulls to the component toward the center of the pad once it touches on the printed solder. It is helpful that the volume rate of the metal occupies half of the volume of the printed solder cream as a rule of thumb. It is interpreted that stencil aperture of 50% of land size in our case can make 1mil thick solder layer above the component lands if it is evenly distributed.

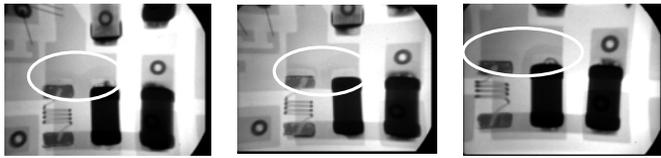
E. PCB MANUFACTURER

The PCB of RFPA module needs very sophisticated lamination, plating and etching technology to guarantee the strict module packaging requirement as well as RF electrical

performance. PCB manufacturers who are better able to control their processes and eliminating process related problems, are those who will need to close relationship with RFPA manufacturers.

IV. RELIABILITY PERFORMANCE

To evaluate the reliability performance with our approach and considerations, three kinds of MSL conditions were evaluated; MSL3 at 240°C/260°C, MSL2 at 240°C separated by A,B groups. The B group which is our final evaluation, did not shows any Solder Extrusion/Flow phenomena regardless of experimented MSL level and temperatures, while A group shows some solder flow phenomena on the weak points but no Solder Extrusion phenomena(Fig.9 & 10).



(a) MSL3 at 240°C (b) MSL3 at 260°C (c) MSL2 at 240°C
 Fig.9 X-ray photo shows Solder Flow phenomena on the weak points – Group A (Interim evaluation group)

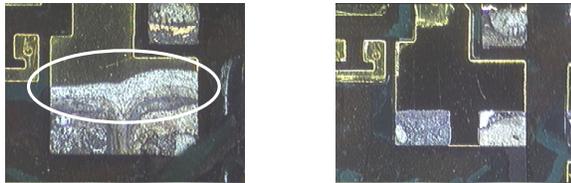


Fig.10 Microscope image after mechanical decapsulation ; Left(Group A) – The photo shows Solder Flow around the component pad (Mechanical decapsulation result of Fig.9 (a)), Right(Group B) – No Solder Flow on the weak points

With the right approach and considerations of critical factors on MSL and Solder Extrusion/Flow, the package reliability and MSL level improvement was accomplished through this study. But, there’s possible extrusion and flow failure if the process, material and design have been changed without any appropriate control. It is sure that the critical factors like process, material and design should be controlled and applied properly.

Conclusions

Significant thermal and moisture stressing cause a diverse list of package integrity failures. To minimize any damage caused by high temperature, not only the treatment of the reflow method but also moisture treatment is the most important besides controlling critical factors and properties. From the standpoint of Solder Extrusion/Flow, MSL2 package integrity have been accomplished through the approach and considerations of critical factors.

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