

Keynote Speeches

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Over the past 10 years, there have been some dramatic changes in the electronics industry. These changes have been spurred by technology, global competitiveness and market demands. The result has been a new interpretation of the discipline of reliability and the role of the reliability engineer in the development of electronic products and systems. This paper overviews the changes that have occurred and how reliability engineering must change to keep pace with the changes and add value to the product development process

1. The History of Electronics Reliability Engineering

Product and system reliability emerged as an identified engineering discipline in the late 1940's. This does not suggest that engineers and designers did not always strive for reliable designs. Engineers have naturally designed and operated equipment to "succeed" and they typically did so by providing a margin of strength over the anticipated loads (stresses). For example, in 1860, A. Wohler presented some of the earliest fatigue failure information, which occurred on stagecoach and railroad axles. The *S-N* (applied load versus cycles to failure) diagrams, which resulted from Wohler's work, were used to identify the load condition, called a fatigue limit, below which "no failures" should be expected.

Reliability engineering for electronics started with the establishment of the Ad Hoc Group on Reliability of Electronic Equipment on December 7, 1950, and the subsequent Advisory Group on the Reliability of Electronic Equipment (AGREE) formed by the U.S. Department of Defense in 1952. One of the first reliability handbooks was titled "Reliability Factors for Ground Electronic Equipment" published in 1956 by McGraw-Hill under the sponsorship of the Rome Air Development Center (RADC). This publication contained information on design considerations, human engineering, interference reduction, and a section on reliability mathematics. Failure prediction was mentioned as a topic under development.

Reliability prediction for electronics is traced to November 1956 with publication of the RCA release TR-1100, titled "Reliability Stress Analysis for Electronic Equipment," which presented models for computing rates of component failures. This was also the first formal publication in which the concept of activation energy and the Arrhenius relationship were used in modeling electronic component failure rates. This publication was followed by the "RADC Reliability Notebook" on October 30, 1959; a report titled "Reliability Applications and Analysis Guide," by D. R. Earles of the Martin Company, in September 1960; and a report titled "Failure Rates," by D. R. Earles and M. F. Eddins, of AVCO Corporation, in April, 1962.

In December 1965, the U. S. Navy introduced the first reliability prediction handbook for electronics, Mil-Hdbk-217A [20]. In this first version, there was only a single point failure rate of 0.4 failures per million hours for all monolithic integrated circuits, regardless of the materials, the design, the manufacturing processes or the life cycle conditions (environment and usage). This single-valued failure rate was illustrative of the infancy of the reliability models, and the fact that accuracy was less of a concern than standardization to the U. S. Department of Defense¹.

In July 1973, RCA proposed a prediction model for microcircuits, based on previous work by the Boeing Aircraft Company. The proposed model consisted of two additive portions: one reflecting a steady-state-temperature-related failure term, and the second a mechanical-related failure term. It was clear to RCA researchers, that any reliability model should reflect device design and fabrication techniques, materials, and geometries. Unfortunately, this attitude was not shared by the RADC, who greatly simplified the models and assumed an exponential failure distribution. This model was then published as Mil-Hdbk-217B under the preparing activity of the Air Force. The exponential distribution assumption still remains in many handbooks today, in spite of overwhelming evidence suggesting that it is often not appropriate [4].

Rapid improvements and increased complexity of microelectronic devices pushed the application of Mil-Hdbk-217B beyond reason. For example, at that time the calculated MTBF for the commonly used 64K RAM was 13 seconds [5]. As a result of this type of incident, on April 9, 1979 Mil-Hdbk-217C [73] was published to "band-aid" the problems. Although Mil-Hdbk-217C was updated to Mil-Hdbk-217D [40] on January 15, 1982, to Mil-Hdbk-217E on October 27, 1986 [12], and to Mil-Hdbk-217F [6] in December 1991, the handbook could never keep up-to-date with the technology advances; the field data took too long to collect and the models could not be extrapolated because they were not based on sound engineering fundamentals. Up-to-date collection of the pertinent reliability data is in itself a major undertaking, especially when manufacturers make rapid improvements in the manufacturing process. As an extreme example of this

¹ Stemming from a perceived need to place a figure of merit on a system's reliability, U.S. government procurement agencies sought standardization of requirement specifications and a prediction process. Without such standardization the military was concerned that each supplier would develop their own predictions based on its own data, and it would be difficult to evaluate system predictions against requirements based on components from different suppliers or to compare competitive designs for the same component or system. Thus, even though the values calculated from the models were unrealistic and often orders of magnitude in error, the erroneous view was that there was commonality between trade-off evolutions.

concern, it has been noted [50] that the connector models in Mil-Hdbk-217 have not been updated for at least 20 years, and were formulated based on data at least that old.

In the last version of Mil-Hdbk-217, two teams were under contract to provide guidelines for this version F update. The University of Maryland (CALCE Electronic Products and Systems Center) and Westinghouse team developed reliability models for advanced technology microelectronic devices to include high gate count devices such as VHSIC, VLSI, and complex packaging approaches such as surface mount, ASIC, and hybrids. Upon completion of the study, they suggested: 1) that the constant failure rate model not be used; 2) that some of the individual wearout failure mechanisms (i.e., electromigration and time-dependent dielectric breakdown) be modeled with a lognormal distribution; 3) that the Arrhenius type formulation of the failure rate in terms of temperature should not be included in the failure model; and 4) that load conditions such as temperature change and humidity be considered. In particular, the University of Maryland-CALCE EPSC/Westinghouse study noted that temperature cycling was becoming more detrimental to component reliability than the steady-state temperature at which the device is operating, so long as the temperature is below a critical value. This conclusion was further supported by subsequent National Institute of Standards and Technology (NIST) study [2], and an Army Fort Monmouth [1] study, which stated that the influence of steady-state temperature on microelectronic reliability under typical operating changes was being inappropriately modeled by an Arrhenius relationship².

In 1994, the U.S. Military Specifications and Standards Reform initiative decreed the adoption of performance-based specifications for acquiring weapons systems, leading to the cancellation of many military specifications and standards [61]. In February 15, 1996, the Army announced that: "Mil-Hdbk-217, Reliability Prediction of Electronic Equipment, is not to appear in an RFP (request for proposal) as it has been shown to be unreliable and its use can lead to erroneous and misleading reliability predictions [7]." In 1997, General Motors and other companies, which formerly used these types of handbooks, concurred with the findings and policy revisions of Feb. 15, 1996, and "Therefore: Mil-Hdbk-217, or a similar reliability assessment method such as SAE PREL, SHALL NOT BE USED." [8] The last modification of Mil-Hdbk-217, Revision F Notice 2 was released on February 28, 1995 and an updated version will not be released. While it is generally believed that reliability predictions can aid in product design and development, the integrity and auditability of many reliability prediction methods were found to be questionable; in that, the models do not predict field failures,

² Reliance on the Mil-Hdbk-217 temperature models proved costly. For example, the use of Mil-Hdbk-217 upfront in the design process, led to design decisions, which maximized the junction temperature in the F22 Advanced Tactical Fighter electronics to 60°C and in the Comanche Light Helicopter to 65°C. In fact, 125°C might have been acceptable and could have resulted in substantial improvements in life cycle cost, weight, volume, support, and reliability. Furthermore, (cooling temperatures as low as -40°C at the electronic's rails were required; to obtain the specified junction temperatures) the resulting temperature cycles are known to precipitate many unique failure mechanisms [42].

cannot be used for comparative purposes, and present misleading trends and relations. However some manufacturers of electronic components, printed wiring and circuit boards, and electronic equipment and systems, still subscribe to Mil-Hdbk-217 type reliability prediction methodologies, although sometimes unknowingly. For example, the Mil-Hdbk-217 approach is common to various reliability prediction procedures³, including: Bellcore TR-TSY-000332, Reliability Prediction Procedure For Electronic Equipment [13], now called Telcordia Technologies Special Report SR-332 [51]; British Telecom, Handbook of Reliability Data for Components Used in Telecommunications Systems [14]; Nippon Telegraph and Telephone Corporation, Standard Reliability Table for Semiconductor Devices [15]; Recueil De Donnees De Fiabilite Du CNET (Collection of Reliability Data from CNET), Centre National D'Etudes des Telecommunications (National Center for Telecommunication Studies) [16]; Siemens AG, Siemens Company Standard SN29500, Reliability and Quality Specification Failure Rates of Components [17]; and PRISM [18].⁴ In fact, on a review of reliability prediction procedures, it was noted that these handbooks derive from some predecessor of Mil-Hdbk-217, the first version, which appeared in 1965 [19]-[20]. The original methodology used in developing the Mil-Hdbk-217 and its progeny has been reviewed in several studies and they are found to lack scientific merit, consistency, and ability to provide design guidance [44]-[49].

2. Changes in Electronics Reliability Engineering

With the passage of time, most of the high-tech electronics companies abandoned the Mil-Hdbk-217 methods including Telcordia and PRISM.⁵ Microelectronic devices were changing too rapidly and the failures were found to follow a time-dependent, rather than constant, failure rate curve that often decreased with time until wearout occurred [29]-[34]. The thermal activation energies for the infant population suggested that temperature had little impact on infant mortality and even after a burn-in screen at elevated temperatures prior to shipment, an installed population of devices might exhibit some infant mortality failures in the first year or so [29]. Fortunately, infant mortality failures are typically due to "mistakes" made during manufacture, and they tend to affect only a subpopulation of shipped product [24]-[27], [41]. Presumably, improved manufacture could significantly reduce the incidence of such failures.

³ Mentor Graphics Corporation, Wilsonville, OR, studied the availability of CAD tools for electronic reliability assessment from the following companies/products: Management Sciences, Inc.; System Effectiveness, Inc.; Power Tronics, Inc.; Item SoftWare, Ltd.; Advanced Logistics Developments, Ltd.; Innovative Software Designs, Inc.; Technicomp, Inc.; Dynamic Soft Analysis, Inc.; and Rome Laboratory products, including RL-Oracle, R&MAT, REST, FASTER, RAMP, and PRISM, and noted that these CAD tools are all Mil-Hdbk-217 based failure predictions.

⁴ Dr. Pradeep Lall (Motorola) found that PRISM was actually a disguised version of Mil-Hdbk-217, which maintained all its disadvantages.

⁵ The traditional (Mil-Hdbk-217 and progeny) approach to predicting the reliability of products in field use, involves implementing using the exponential, or constant failure rate, statistical models based primarily on field data [11].

Wearout failures, by contrast, relate to mechanisms that affect the entire population. When modeled using physics-of-failure methods, wearout mechanisms could be "designed out," with the result that wearout failures were no longer likely to occur during the normal service life of microelectronic devices [21] -[23] , [28] -[38] . The reliability goal today is focused on damage assessment techniques whereby the root causes of failure are assessed, detected and corrected [9] - [10] .

An overview of the key reliability tasks and the reliability inputs necessary in much of today's product development is given below.

Product Design for Reliability: Reliability assessments are often used to define the attainable minimum needs for product success, based on the life-cycle application. From this, a reliability goal may be made to serve as a minimum requirement for the "deliverable reliability. These requirements can then guide tradeoffs in the initial product development, such as supply chain creation, part selection and redundancy.

Reliability assessments must be based on physics of failure principles when selecting and comparing alternative parts and designs, in order to model the actual products.⁶ It is generally too late to make trade-offs if it necessary to collect field data. For example, because Mil-Hdbk-217F and progeny methods require field data for model development, one would select ECL for high-speed and high-reliability applications over Bi-CMOS, when in fact Bi-CMOS is now a mature and more highly reliable technology.

Load and Stress Analysis: Given the system parts and design, reliability assessment models are used to assess the influence of the life cycle condition (manufacture, assembly, transportation, handling, operating, maintenance, etc.). This provides input to environment-controlling systems (i.e., vibration and cooling systems) and derating techniques. Temperature, humidity, electrical fields, vibration, and radiation are example conditions affecting reliability.

Derating: Derating is based on the concept that operating electrical, thermal-mechanical and chemical "stresses" accelerate failures in a predictable manner, which if controlled, will improve reliability. For electronics, typical derating parameters include current, voltage, power, fanout, frequency, and operating (i.e., junction) temperature. Using the mathematical expressions of reliability prediction, one can often derive a derate schedule. Such schedules must be based on the dominant failure mechanisms for the particular electronics and must include the mechanical and structural elements, and device interactions, as well as the devices themselves.

Environmental Controls: There are various ways in which both the operating and environmental loads (stresses) can be controlled to improve reliability. Methods can be applied directly to the system to keep harmful conditions (i.e., high and low temperatures, temperature cycles, high shock loads,

high humidity, high radiation) away from sensitive devices and structures. Methods can also be applied to control the operation and/or manage the system environment to limit load conditions.

The cost and complexity of load control must be balanced against reliability factors associated with the load control. For example, steady-state temperature is often considered a major reliability factor, and much effort goes into lowering the temperature of the electronics. Although the traditional reliability prediction methods provide a model relating steady-state temperature to reliability, studies have shown that these relations are generally false [1] -[4] . Any apparent agreement between elevated temperatures and high failure rates should not necessarily lead to the conclusion that steady-state temperature is the cause of the failures, when in fact, temperature cycling may be the culprit. [42] -[43]

Screening: Screening is the process by which defective parts, resulting from improper or out-of-control manufacture and assembly processes are detected and eliminated from a production batch. The principle involves inducing failures only in a population that already has "weak" parts, without reducing the reliability in the population of "strong" parts. The assumption is that through the application of short-term stresses, failures in the weak population can be precipitated, leaving a highly reliable population. Stress screening and burn-in (i.e., high-temperature screen) methods should not be based on reliability prediction models, but on acceleration stress levels that are often derived from the models for the potential failure mechanisms associated with potential problems in quality.

One type of screen is called burn-in, whereby the parts are operated for a period of time at high temperatures in order to precipitate defects, and hence failures, in the weak population of parts. For parts with low failure rates (i.e., below 10 failures per million device hours) Motorola noted that burn-in prior to usage does not remove many failures. On the contrary, it may cause failures due to handling [3] . In fact, even the preparing agency for the most common electronics parts screening document, Mil-Std-883, stated that: "These end-of-line screens (Mil-Std-883) provide a standard series of reliability tests for the industry. Although manufacturers continue to use these screens today, most of the screens are impractical or need modifications for new technologies, and add little or no value for mature technologies." [39]

Failure Modes, Effects and Criticality Analysis (FMECA): FMECA is a method to assess the interoperability of the parts, subassemblies, assemblies, and subsystems comprising the system. The objectives are: to determine the effects of failures on system operation; to identify the failures (especially "single-point" failures) critical to operational success and personnel safety; and to rank each potential failure according to the effects on other portions of the system, the probability of the failure occurring, and the criticality of the failure mode. Reliability predictions are often used to determine the probability of failure for each potential failure mode of each element in the system.

Maintainability and Logistics: Maintainability assessment often uses failure rate data from reliability prediction models

⁶ Individual parts must not be considered to be the only, or necessarily the major, source of failures. Interconnections and system interactions are also sources.

to determine a mean-time-to-repair (MTTR) from sub-system times-to-repair. The MTTR and metrics associated with acquisition, personnel, business, and other issues are then used, along with reliability predictions, to calculate logistics parameters such as availability and supportability. It is critical that the design team realizes that errors in the reliability predictions can be multiplied many times in the calculation of logistics metrics.

Certification: This is the culmination of the product development process, where it is agreed that the product is ready to be introduced to the market, having met or exceeded marketing, contractual, regulatory, or other goals for performance. Reliability is often an item affecting the final decision to enable product operation.

Warranty: The expectations of reliability often affect the warranty terms. In some cases, suppliers may be required only to meet contractual goals without incentive for, or interest in, continued reliability improvement. That is, the concept of "attainable maximum" often provides an easily achieved cap on expectations. There are many other warranty arrangements, often intended to encourage suppliers to treat product reliability seriously. For example, the desired reliability goal bears economic considerations that affect life-cycle cost. Those costs are usually included in the fundamental economic analysis to determine economic feasibility of the total program, and in some cases can be an important item in total costs of ownership.

Failure Diagnosis and Corrective Actions: Failure diagnosis and corrective actions are key to continuous product improvement. When the goal is only to meet warranty requirements, there is seldom any interest in further diagnosis and corrective action after the goal has been met. In such an instance, reliability prediction may provide the basis for a hindrance to continued improvements in reliability. Reliability growth is associated with the continuous improvement in product reliability [4]. However, once again, the calculated reliability should not necessarily be considered to be the maximum achievable reliability.

Cost Effectiveness: Many variables affect cost effectiveness, the materials, weight, volume, dependability, and a myriad of other factors can all have a role, and thus cost effectiveness studies can be quite complex. For example, with aviation equipment, dollar cost can be less significant than other factors such as weight, volume, and power consumption and all costs must be defensible in terms of product value.

3. Challenges For Electronics Reliability Assessment

In an effort to develop reliable electronic products in a rapidly changing global market an auditable reliability assessment methodology must be established; one which accounts for the materials, design, manufacturing processes, and specific application of the product. Furthermore, because the timely delivery of products is critical to cost-effectiveness and competition, the techniques of the methodology must be executable in an efficient manner. Some of the key challenges today include:

- Development and use of electronic part selection and management techniques that ensure that parts, which are compatible with the life cycle of the product, are

used is a current research concern. [52] -[66] Reliability assessment of parts for application in a specific environment should be performed integrated with the part selection and management process.

- Development and use of appropriate methodology for use of parts outside manufacturer specified temperature limits. The availability of electronic parts rated for operating temperature ranges wider than 0-70°C (commercial temperature range) is decreasing, as semiconductor manufacturers are prone to test and rate parts only in terms of 'commercial' applications (e.g., consumer and computer products). Nevertheless, there is a need for parts requiring a larger operating temperature range, especially in avionics, military, automotive and oil drilling electronics. Up-rating is defined as a process to assess the capability of a part to meet the functionality and performance requirements of the application in which the part is used outside the manufacturers' specification range. The researchers in CALCE electronic products and systems center in collaboration with industrial partners are studying up-rating. [67] -[72]
- Development of physics-of-failure models, an up-front approach to reliability, which utilizes the knowledge of stresses, materials, and structure to identify potential failure mechanisms so as to prevent product failures. A stress refers to the impact of environmental and operating conditions, such as an applied force or an electric field. A failure mechanism refers to the physical process(es) that bring about failure, such as electromigration, corrosion or fatigue. Some of the common failure mechanisms that affect the reliability of electronic products are discussed in a series of IEEE tutorials [74] -[87]
- Transformation of accelerated stress conditions to normal operating conditions for assessment of reliability in normal application conditions. This depends on the availability of physics of failure models and the knowledge of what product characteristics influence the models [88] -[92].
- Assessment the results of tests that are re-test ok or error-not-found (could not duplicate). This is a matter of major concern for industries that replace items on warranty and then to identify the failure cause for the failed products.
- Development of mixture models which consider both early and premature wear-out failures caused by the displacement of the mean and variability due to manufacturing, assembly, handling, and misapplication.
- Development of multiple-event and repeated failure models that address the problems in lifetime distributions and repairable systems.

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Prospects of System IC Semiconductor Industry

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Extended Abstract

The current semiconductor downturn we are witnessing is primarily caused by the downturn of IT industry starting from the later part of year 2000. The semiconductor business performance of year 2000 was exceptionally good, which resulted in an aggressive industry-wide capacity expansion. As both corporate and consumer's demand for PCs and IT infrastructures such as servers and network equipments got softened along with the weak demand for mobile phones in conjunction with the slow-down of the economy, the down-turn cycle of this semiconductor business seemed to have lasted longer into an L-shaped curve rather than a V-shaped one. Looking back last 40 years, it has been a well-known fact that the semiconductor business has a typical cyclic nature. However, the important factor is that it has been a continuously growing industry.

In this talk, three areas of topics will be covered. The first is the market prospects. The second is the technology prospects, and the last will be the direction of Korea semiconductor industry in the future.

Market Prospects: The PC has been the major driving force of the semiconductor market growth for both DRAM and logic chips. As the PC market gets saturated and demand slows down, we expect that the demand from alternative applications such as mobile phones and Internet and digital appliances will grow. These new post-PC applications will drive higher density, low power technology because of the needs for mobile applications. We will identify the future applications emerging as alternatives to PC as new source of market demand to drive the volume.

Technology Prospects: The speed of semiconductor development for performance and density has been successfully following the Moore's law, which means that the performance of CPU or density of memory chips doubled every 18 months. So, the development speed has been exponential. How will the Moore's law work for the development of the semiconductor industry for the next ten years? We will look for the answers from aspects of semiconductor's deep sub-micron process technology development, design technology for large-scale system chips, and manufacturing technology. Technical challenges and limitations in each area will be identified with discussion of potential solutions.

Korea Semiconductor Industry Prospects: Thanks to the "select and focus" strategy, the Korea semiconductor industry has achieved the leadership position in the world DRAM market by having more than 40% worldwide market share as of today. However, the downside of today's Korea semiconductor industry is heavy dependency on

DRAM. The memory covers 85% out of total semiconductor production in Korea while memory products cover only 25% of the worldwide semiconductor market. Presently, the Korea semiconductor industry is paying more attention to the development of non-memory side semiconductor, so called system IC business, as a way to mitigate the volatility of DRAM business caused by highly cyclic business nature and also to support the growing system business such as mobile communication and digital appliance products. The near term goal of Korea semiconductor industry is to achieve balanced business portfolio by having the revenue mix of 50% and 50% between memory and system IC business. Unlike memory products, system IC has very wide range of products spanning from simple devices to system level chips, and the required skill set for the industry is different. The current status and future development direction of Korea system IC industry will be presented.

Overview of Recent Developments in Microelectronic Packaging

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The total output of the world wide electronic industry has exceeded one trillion dollars. This industry has been growing at more than ten percent per year over the last quarter of a century. The growth of this industry has been propelled by two major factors: the innovation and advancement in semiconductor and packaging technologies, and market pull for electronic products from all segments of the industry. The advancement in semiconductor technology has been well described by Moore's Law, which states that transistor density double every three years. This rate of innovation and progress in semiconductor manufacturing led directly to the major trends for the electronic industry, which are increasing miniaturization, faster performance, and broadening application. The key enabler for success of semiconductor technology in the electronic industry market place is microelectronic packaging technology. Packaging has advanced with IC devices in locked steps providing the powerful and cost effective electronic components to the computer, medical, telecommunication, consumer electronics, automotive, and other industries.

This presentation will review recent developments and future challenges in microelectronic packaging. The increase in transistor density per each generation of semiconductor technology results in demands for corresponding increase for packaging interconnection density. In meeting these demands there has been a continuous stream of new innovations and new developments in all aspects of microelectronic packaging: in materials, processing, new designs, reliability and testing, metrology, modeling and simulation.

Wirebond pitch has continued to lower. While a few years ago one might think the minimum practical limit was at about 50 to 45 μm , the thinking today is that the industry will reach 20 μm in 5 to 7 years. While flip chip infrastructures were limited to a few large integrated semiconductor companies, high volume bumping foundries and assembly service providers have emerged to meet the industry needs for high I/O capabilities at 1000 I/o and more. At the same time the area array solder bump pitch will be at 200 μm and below.

In response to the dramatic changes underway in the computer, telecommunication, health, transportation, and consumer electronics industries, new concepts in BGA, and CSP designs have emerged to meet the diverse application requirements. For example QFN and BCC packages are smaller and thinner with lower inductance particularly suitable for the wireless applications. Stacked chip package provides a small profile and low cost package to meet particular functional requirements. Wafer level CSP packages have found applications in integrated passives and other small devices.

The high I/O trend at the IC level leads to high interconnect density requirement at the substrate level. The industry is being challenged to provide substrate solutions in high volume for devices with 2-3000 I/O and more at 200 um pitch and less.

Materials and materials processing has been the key element for new package development and package reliability. Solder and underbump metallurgy interaction have been shown to be critical in solder bump electromigration. Surface condition and surface modification are important for interface integrity for MSL 1 and 2. It has been estimated that materials occupies a large fraction of a package cost. The knowledge of materials and the use of materials will continue to be of critical importance as we progress from 130 nm technology to beyond.

A Mechanical Reliability Assessment of Solder Joints

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Abstract

A mechanical reliability of the solder joints is a serious concern. Intermetallic compounds are formed during reflow process between solder and electrical pads and gradually grow in service. Due to its brittle manner, the reliability of solder joints are supposed to degenerate. By using the Cu-plates on which Cu or Ni or Ni+Au plating was deposited, and solders (Sn-Pb solders or Sn-Ag-Cu solders), the specimen of solder joints were fabricated. After aging it in an isothermal chamber, tensile tests were performed and the relationships between solder joint strength and aging period were considered. From SEM microscope observation and EDX microprobe analysis, the growth and components of the intermetallic compounds layer were examined. To investigate the stress condition on the solder joint interface, the finite element analysis was also carried out.

Introduction

Recent trend of significant reduction of solder bump size leads to sever requirements for mechanical reliability of the solder joint as compared with before[1-3] and the assessment of the mechanical reliability become an important issue.

Metallurgical interactions occur between the solders and other materials by means of solid state processes and resulting reaction products (intermetallic compounds, IMC) will continue to grow as the solder joint ages. The formation of a thin layer of the intermetallic compound is considered desirable for achieving a good metallurgical bond at the interface. However, due to its brittle nature and lattice mismatch, the solder cracks tend to be generated near the intermetallic compounds [3]. Formation of these intermetallic compounds affects the mechanical integrity of solder joints [4-7]. Therefore it is important to study the effect of intermetallic compounds on the mechanical properties of the solder joints.

The lead-tin(Pb-Sn) solder alloy has been widely used as interconnection material in electronic packaging due to its low melting temperatures and good wetting behavior on several substrates such as Cu, Ag, Pd and Au. Recently, due to environmental and health concerns, a variety of new Pb-free solders are developed. Pb-free solders lack the toxicity problems associated with leaded solders. However, unlike leaded solders, the recently employed Pb-free solders do not have a long history and manufacturing process and engineering database have not been established. Mechanical properties of Pb-free solder joints have not been clarified. Especially, the influence of intermetallic compounds development on the reliability of the solder joints have not been investigated.

In this study, to investigate the influence of intermetallic compound layer development on the mechanical reliability, tensile tests were performed for the solder joints after thermal aging and the relationships between solder joint strength and aging periods were examined. From SEM microscope observation and EDX microprobe analysis, the growth and components of the intermetallic compounds layer were examined. The development of intermetallic compound layer thickness will influence on the stress condition around the solder joint. To investigate the stress condition on the solder joint interface, the finite element analysis was carried out.

Experimental Procedure

The specimen consists of two copper plates with 0.9 mm thickness, plating layers and solder. The configuration of the test specimen is depicted in Fig.1. The plating layers were composed of Cu or Ni/Cu or Au/Ni/Cu structures. Each layer was grown by electroplating. Cu and Ni layers were 5 μm and Au layer was less than 1 μm thickness, respectively. In this work, Sn-Ag based solders such as Sn3.5Ag0.75Cu, Sn1.0Ag0.5Cu were used. To compare with conventional solders, Pb-Sn based solders such as 63Sn37Pb, 62Sn36Pb2Ag were also used. The stress-strain relations of these solders are shown in Fig.2. The strength of Pb-free solders are smaller than that of Pb contained solders. As the amount of Ag increases, the strength of solder becomes larger. Strips of these solders were put between copper plate and infra-red reflow process which is used in standard surface mount technology (SMT) was carried out for the reflow. The reflow temperatures are shown in Table 1.

To study the solid states growth kinetics of the intermetallic compounds at the solder joints, specimens were placed in the isothermal chamber at 125 degree centigrade for

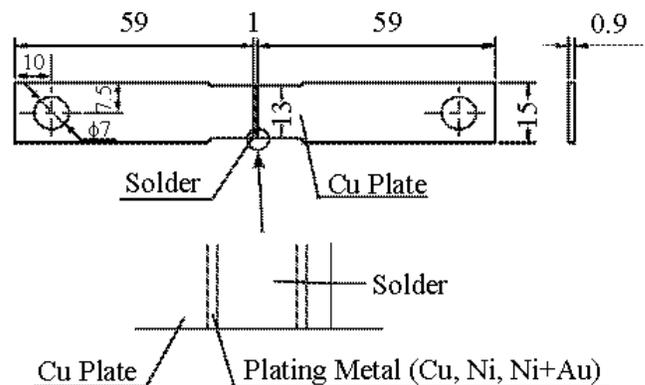


Figure 1. Configuration of the test specimen.

Table 1. Solder types and reflow temperatures.

Solder Types	63Sn 37Pb	62Sn36 Pb2Ag	Sn3.5Ag 0.75Cu	Sn1.0Ag 0.5Cu
Melting Temperature	183°C	170 ~ 190°C	216 ~ 220°C	210 ~ 216°C
Reflow Temperature	240°C	240°C	260°C	260°C
Plating Metals	Cu, Ni, Ni+Au			

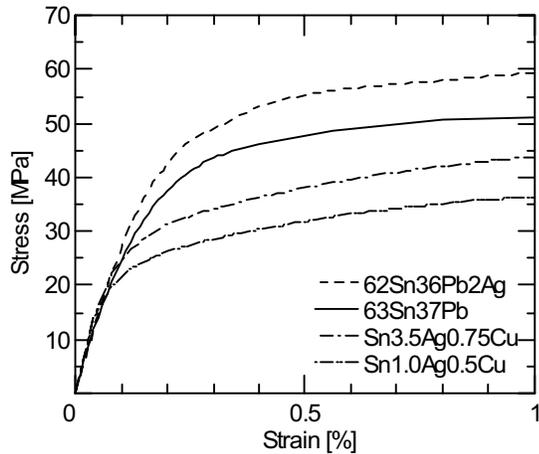


Figure 2. Results of tensile tests.

one to 120 days. After cooling down for one day at room temperature, tensile tests were performed. The tensile load was applied perpendicular to the solder joint layer with cross head speed of 0.5mm/min at 22 degree centigrade. For microstructural observation at the solder joint interface, some of the specimen were sectioned using a low-speed diamond saw and metallographically polished to reveal the interface and the internal microstructure of the solder joints. Microstructural characterization was carried out and the composition of each phase was investigated by EDX microprobe analysis.

Experimental Results

Growth of intermetallic compounds layer

Cross-sectional morphologies of the intermetallic layers in Cu/62Sn36Pb2Ag solder joints annealed for 0 and 80 days at 125 degree centigrade are shown in Fig.3. Back-scattered electron imaging (BEI) was used to obtain the micrographs to produce better contrast among various layers of material. From left to right, the regions in each of these micrographs are the solidified solder, reaction zone, and Cu layer. Intermetallic compounds region can be seen clearly in the 80 days aged specimen. From EDX microprobe analysis, η -phase Cu_6Sn_5 and ϵ -phase Cu_3Sn were found in the reaction zone. Such microstructures of Cu-Sn interfacial intermetallic compounds described above are similar to what other researchers have found in bimetallic couples of Sn-Pb solders

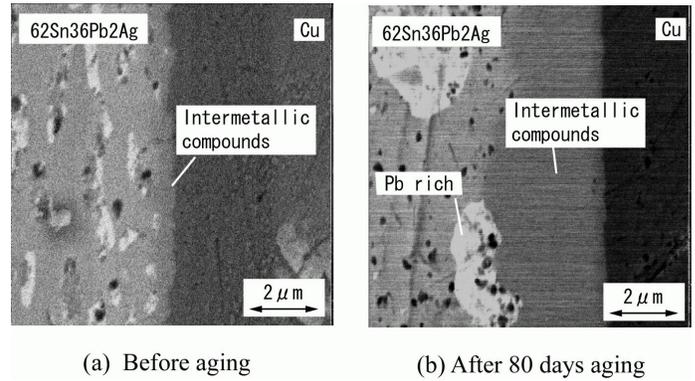


Figure 3. Micro structures of Cu/62Sn36Pb2Ag solder interface.

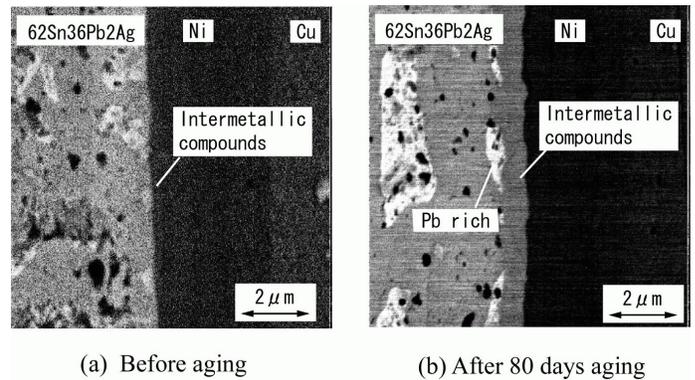


Figure 4. Micro structures of Ni/62Sn36Pb2Ag solder interface.

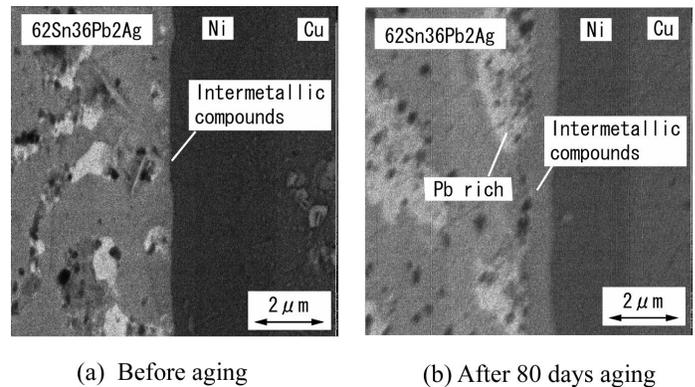


Figure 5. Micro structures of Au+Ni/62Sn36Pb2Ag solder interface.

on copper [8]. The formation of η -phase Cu_6Sn_5 intermetallic layers in solder joint during the reflow process arises by interfacial reactions between its constituting species, Sn from the solder and Cu from the copper plate. During isothermal aging, the η -phase Cu_6Sn_5 in IMC layer grows by interdiffusion of Cu and Sn and reaction with each other, while the ϵ -phase Cu_3Sn forms and grow by reactions between the Cu substrate and η -phase Cu_6Sn_5 layer.

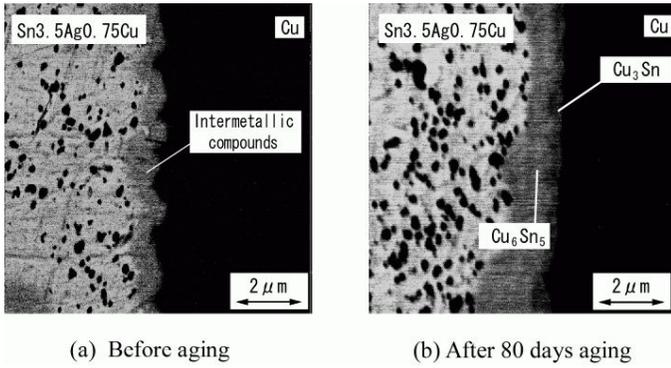


Figure 6. Micro structures of Cu/Sn3.5Ag0.75Cu solder interface.

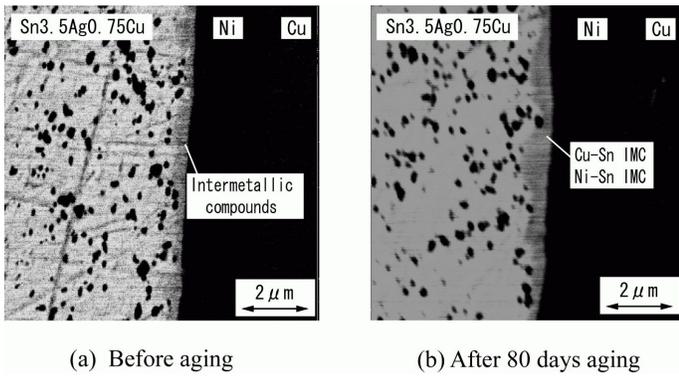


Figure 7. Micro structures of Ni/Sn3.5Ag0.75Cu solder interface.

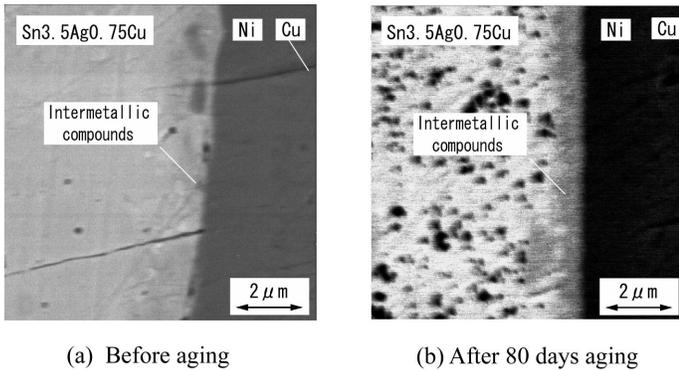


Figure 8. Micro structures of Au+Ni/Sn3.5Ag0.75Cu solder interface.

Furthermore, Pb-rich phases were euduced adjacent to the intermetallic compounds due to the migration of Sn from solder to the reaction zone.

Ni metallization is commonly used as a protective layer on a Cu conductor in electronic devises and circuit fabrications. This layer provides a diffusion barrier to inhibit detrimental growth of Cu-Sn intermetallic compounds. Interfacial reaction between 62Sn36Pb2Ag and Ni plating layer is depicted in Fig.4. Ni/62Sn36Pb2Ag solder joints were

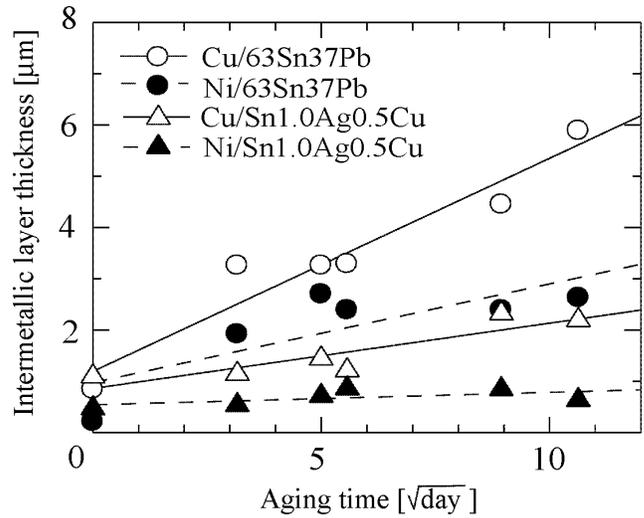


Figure 9. The development of the intermetallic compound layers.

aged for 0 and 80 days at 125 degree centigrade. From left to right, the regions in each of these micrographs are the solidified solder, reaction zone, Ni layer and Cu layer. Intermetallic compounds formed between Ni plating and the solder and can be seen clearly in the 80 days aging specimen. The Pb-rich phases were euduced adjacent to the intermetallic compounds layer like Cu plating case. The thickness of intermetallic compounds is thinner than that of Cu plating case. From EDX microprobe analysis, intermetallic compound layer was composed of Cu-Sn and Ni-Sn compounds. These compounds were mixed in intermetallic compounds layer and could not be distinguished clearly.

The Au/Ni/Cu three layer structure is one of the most common solder ball pad finishes for the ball-grid-array (BGA) packages. Interfacial reaction between 62Sn36Pb2Ag and Au+Ni plating layer is shown in Fig.5. Au+Ni/62Sn36Pb2Ag solder joints were aged for 0 and 80 days at 125 degree centigrade. From left to right, the regions in each of these micrographs are the solidified solder, reaction zone, Ni layer and Cu layer. The Au layer could not be identified here. Intermetallic compounds region can be seen clearly in the 80 days aged specimen. The Pb-rich phases were euduced adjacent to the intermetallic compounds layer like the previous cases. The thickness of intermetallic compounds is almost equal to Ni plating case. From EDX microprobe analysis, intermetallic compound layer was composed of Cu-Sn and Ni-Sn compounds. As similar to Ni plating case, these compounds were mixed in intermetallic compounds layer and could not be distinguished evidently.

In Au+Ni plating cases, the Au layer could not be identified from the SEM observation and could not be detected by EDX analysis. From the recent study of Kim and Tu[9], Au reacts rapidly with molten Pb-Sn solders to form AuSn₄. This reaction was extremely fast. At 200 °C, the AuSn₄ layer could grow to 10 μm thick in 5 sec. During the fabrication of the specimen, the Au layer dissolved into the solders very quickly and the Ni layer was exposed. The exposed Ni reacted with the solder to form Ni-Sn compounds

at the interface. Therefore, the composition of intermetallic compounds layer is similar to that of Ni plating case.

Figures 6-8 show the cross-sectional morphologies of Sn3.5Ag0.75Cu solder joints treated by each metallization. The aging periods are for 0 and 80 days at 125 degree centigrade. Intermetallic compounds region can be seen clearly in the 80 days aged specimen. Since this solder is Pb-free type, Pb-rich phases could not be seen on the interface. The thickness of intermetallic compound layer is thinner than that of 62Sn36Pb2Ag solder joints for every plating cases. The composition of intermetallic compound layer is similar to 62Sn 36Pb2Ag solder joints.

The thickness of intermetallic compounds layers for 63Sn-37Pb solder and Sn1.0Ag0.5Cu solder with Cu or Ni plating case is depicted in Fig.9. From this figure, the thickness of intermetallic compounds layers increase in proportional to the square of aging period. The thickness of intermetallic compounds layers of Pb contained solder is larger than that of Pb-free solder. The reaction rate of Ni and Sn is slower than that of Cu and Sn. For the Pb free solder joints with Ni plating, the intermetallic compounds thickness is almost constant during this aging period. Intermetallic compounds layer was formed at reflow process stage and it does not influenced by the aging periods under 125°C. This result suggests that, for Pb free solder, the intermetallic compound development can be controlled by using Ni plating pads.

Tensile strength of the aged solder joints

From the results of the cross-sectional morphologies, several kinds of intermetallic compounds layers were formed at the interface. The formation of these compounds seems to affect the reliability of the solder joints. In this study, tensile tests were performed for the solder joints after thermal aging and the relation between intermetallic compounds growth and the tensile strength were investigated.

From the observation of the tested specimen, the fracture pattern can be classified under the three types as shown in Fig.10. Fig.10(a) shows that the fracture occurred between solder and intermetallic compounds layer and Fig.10(b) shows the fracture occurred in the solder itself. Mixed fracture type of these two types is shown in Fig.10(c). Figure 11 shows the relationship between the tensile strength and the thermal aging time for 63Sn37Pb solder case. The symbols using in this figure represent the fracture patterns classified in Fig.10. From this figure, the tensile strength of the Cu plating case is larger than the other plating cases. The tensile strengths decrease with aging period and become constant after the 60 days thermal aging. The decrease rate of the tensile strength for the Cu plating case is slower than the other plating cases. For the Cu and Ni plating cases, fracture occurred in the solder at first and, after some aging period, the fracture pattern changed to the interfacial fracture. On the other hand, the fracture pattern of the Ni+Au plating case was mainly the interfacial fracture. Cu plating pad finishes are preferable for the 63Sn37Pb solder case.

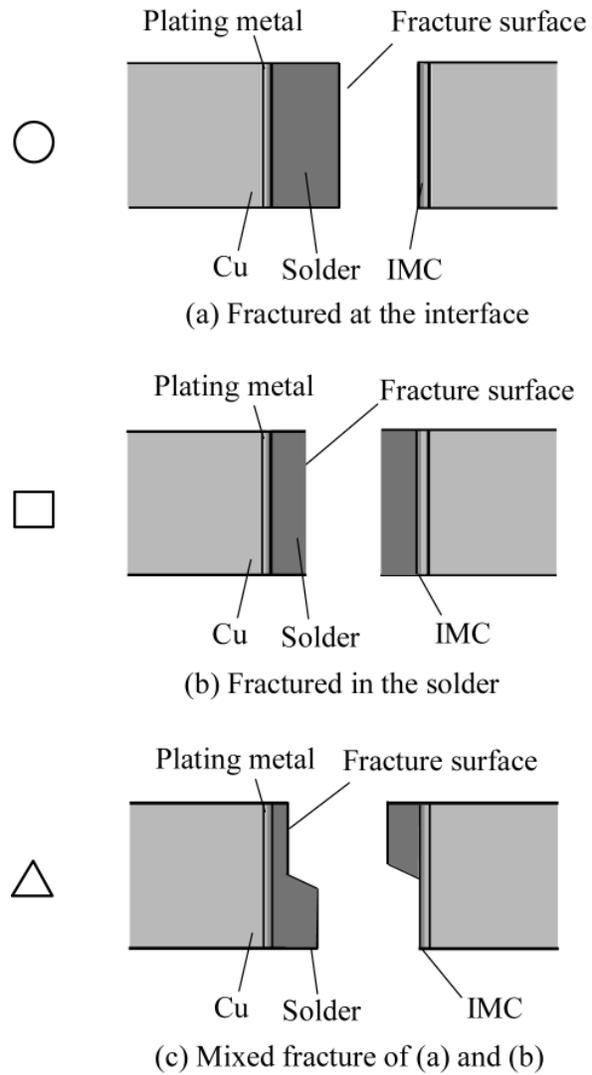


Figure 10. Fracture patterns of the failed specimen by the tensile testing.

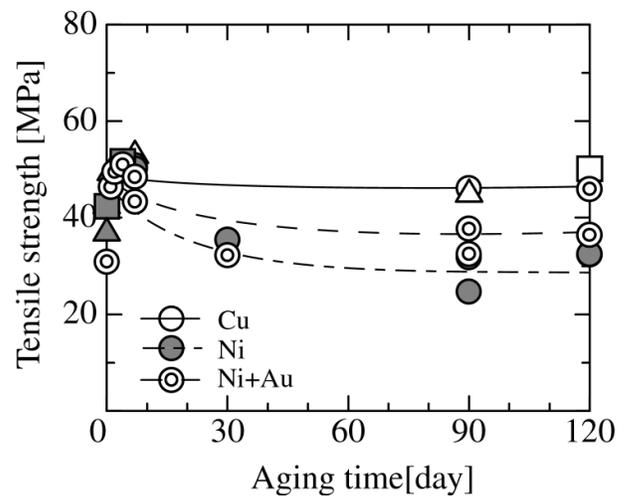


Figure 11. The effect of aging time on the tensile strength for 63Sn37Pb solder case.

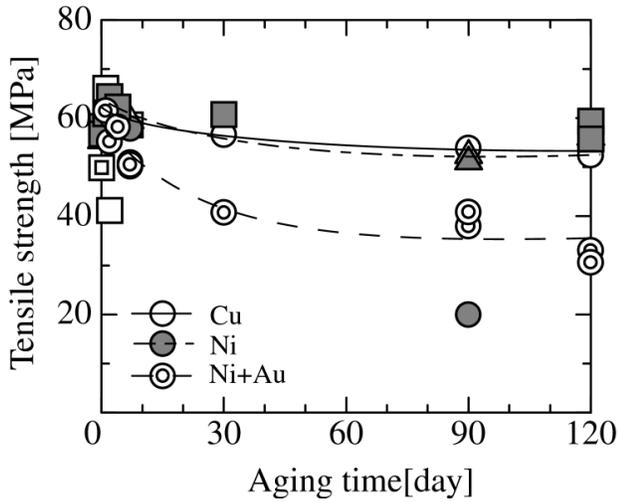


Figure 12. The effect of aging time on the tensile strength for 62Sn36Pb2Ag solder case.

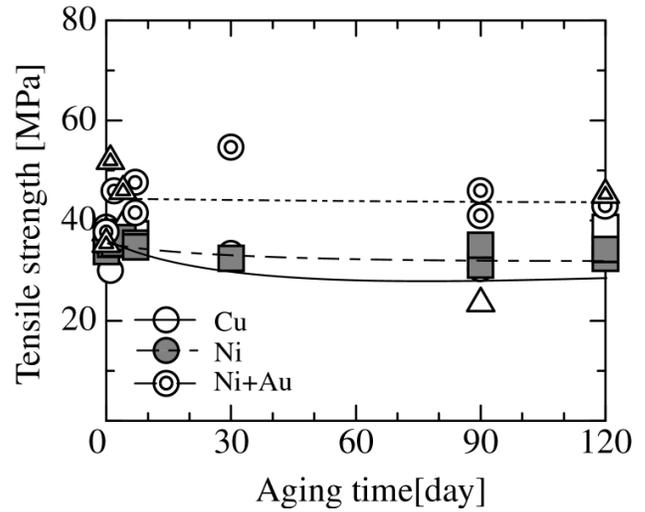


Figure 14. The effect of aging time on the tensile strength for Sn1.0Ag0.5Cu solder case.

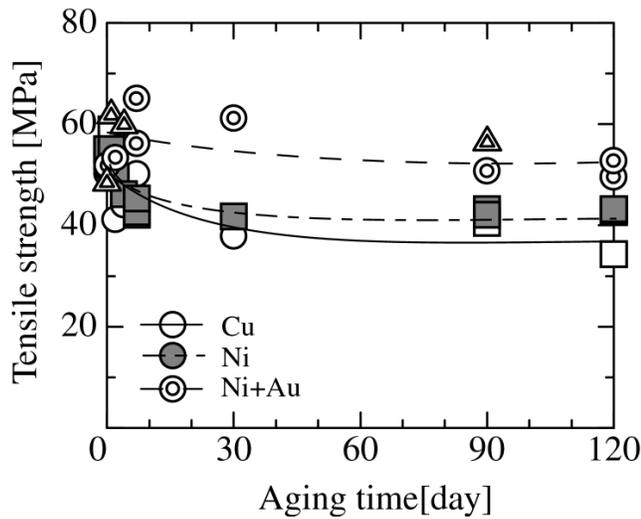


Figure 13. The effect of aging time on the tensile strength for Sn3.5Ag0.75Cu solder case.

Figure 12 shows the relationship between the tensile strength and the thermal aging time for 62Sn36Pb2Ag solder case. From this figure, by adding Ag in the solder, the tensile strength increase for all plating cases. As same as 63Sn37Pb cases, the tensile strengths decrease with aging period and become constant after the 60days thermal aging. The decrease rate of the tensile strength for the Cu and Ni plating case is slower than that of Ni+Au plating cases. For the Cu plating case, fracture occurred in the solder at first and after some aging period, the fracture pattern changed to the interfacial fracture. For the Ni plating case, the fracture occurred in the solder. For Ni+Au plating case, the fracture occurred at the interface. Au coating on Ni plating enhanced the strength of solder itself. This is due to the diffusion of Au into the solder during the reflow process[10]. Cu or Ni plating pad finish is preferable for the 62Sn36Pb2Ag solder case.

For the Pb-free solders, the relationship between tensile strength and aging periods are depicted in Figs. 13 and 14. In contrast with Pb contained solder, the tensile strength of Ni+Au plating case is larger than the other plating cases. As same as Pb contained solder, the tensile strength decrease with aging periods. The decrease rate of the tensile strength for the Ni+Au plating case is slower than the others. Especially, in Sn1.0Ag0.5Cu case, the tensile strength of Ni and Ni+Au plating cases are independent of aging time. The reaction rate of Ni and Sn is very slow. Therefore, the thickness of IMC layer and the surface condition at the interface is not so different during this aging period. Therefore, thermal aging do not affect the tensile strength of Pb-free solders with Ni+Au plating cases. Ni+Au plating pad finishes are preferable for Pb-free solders.

Numerical Analysis

In the experimental results, tensile strength tends to be constant after some aging periods. To investigate this phenomenon, the finite element calculations for Cu/62Sn36Pb2Ag case are carried out by using ABAQUS®(Ver. 5.8). Figure 15 shows the numerical model. There exists the intermetallic compounds layer between copper and solder. The thickness of the intermetallic compound layer increased with the aging periods as shown in Fig.9. The intermetallic compound layer thickness of Cu/62Sn36Pb2Ag case is almost same as that of the Cu/63Sn37Pb case. Therefore, we roughly decided the intermetallic compound layer thickness as shown in Table 2. Material properties of the specimen were referred from the literature[3]. In the numerical calculation, the plane strain condition is assumed and the nominal stress, when the specimen ruptured, is applied at the top of the specimen as the boundary condition. In 270 days case, the tensile strength of 120 days is used because the tensile strength was not so different after 60 days thermal aging. The specimen was in isothermal chamber for the thermal aging under 125 °C and tensile tests were carried out at the room temperature.

Table 2. The thickness of the intermetallic compound layer for Cu/62Sn36Pb2Ag case.

Aging time [days]	0	7	30	90	270
IMC layer thickness t [μm]	1	2	3	5	8

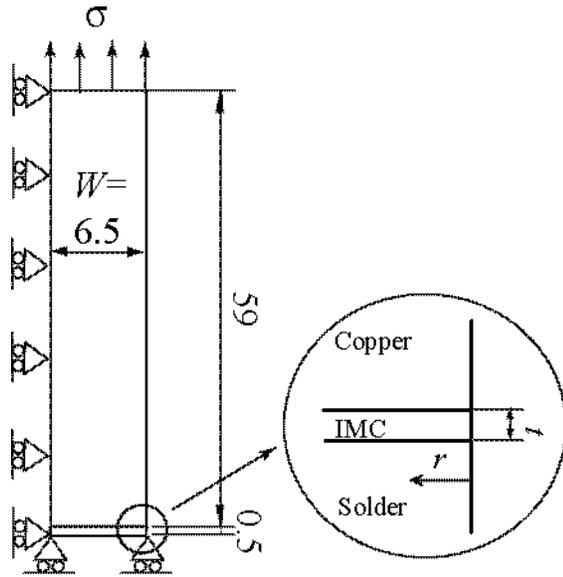


Figure 15. The numerical model for the Cu/ 62Sn36Pb 2Ag case.

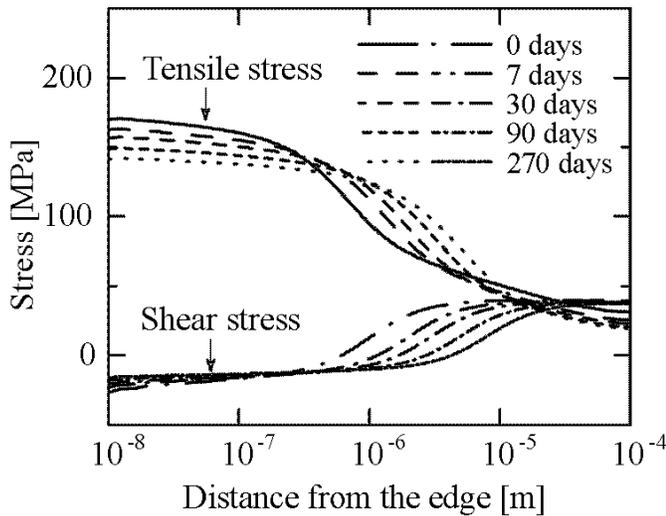


Figure 16. The interfacial stresses on the Copper/IMC interface.

Therefore, the thermal residual stress is also considered in this calculation. At first step of the analysis, the thermal residual stresses were computed by changing the temperature of the

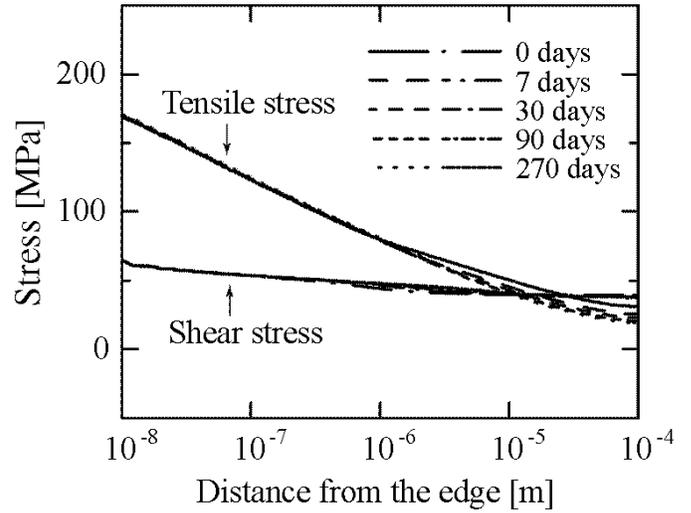


Figure 17. The interfacial stresses on the Solder/IMC interface.

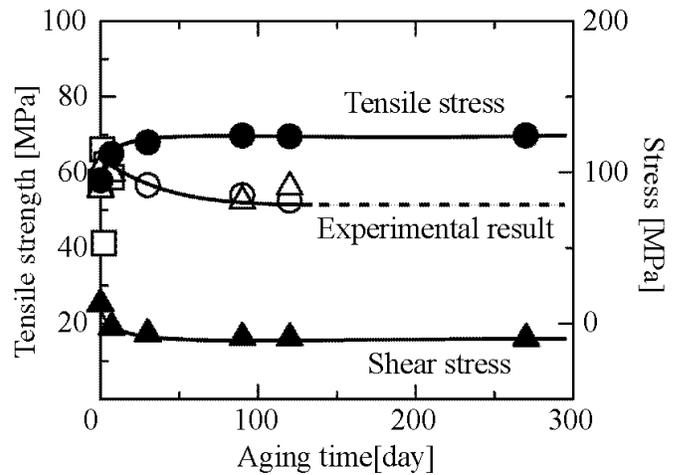


Figure 18. The relationship between the interfacial stresses and aging time.

specimen from 125 °C to 22 °C. And then the nominal stress at failure was applied at the top of the specimen.

The tensile and shear stress distributions on the Copper/IMC interface and the Solder/IMC interface are showing in Figs. 16 and 17, respectively. On the Copper/IMC interface, the stress distribution along the interface is influenced by the aging periods, that is, the thickness of the intermetallic compound layer during the short aging period. The tensile and shear stresses are mixed. However, as the thickness of intermetallic compound layer increase, the shear stress decrease and the tensile stress become dominant. Once the thickness of the intermetallic compound layer develop over the critical thickness (about 3 μm), the stress distributions near the edge become independent of aging period. On the other hand, the stresses on the Solder/IMC interface are not influenced by the intermetallic compound layer development.

Figure 18 shows the relationship between the stresses at 1 μ m for the Copper/IMC interface and the aging periods. The experimental results of failure stress are also depicted. Although the failure stress decrease, the tensile stress at interface becomes a constant and independent of thickness of the intermetallic compound layer. This stress value is considered to be a critical interface strength. This result suggested that the stress based reliability assessments can also be applied to the solder joints subjected to thermal aging and the period of the thermal aging testing can be reduced by combining numerical stress analyses.

Conclusions

In this study, tensile tests were performed for the solder joints after thermal aging and the relations between solder joint strength and aging periods were examined. From SEM microscope observation and EDX microprobe analysis, the growth and components of the intermetallic compounds layer were also examined. For the Pb contained solders, Cu plating is preferable of the Cu pads finishes, since the strength of tensile strength of Cu plating is larger than the other plating cases and is not influenced by thermal aging. On the contrary, for the Pb free solders, Ni+Au plating is preferable of the Cu pads finishes, since the tensile strength of Au+Ni plating is larger than the other plating cases and is not influenced by thermal aging. The finite element analysis indicated that the tensile stress along Copper/IMC interface near the edge become independent of aging period once the thickness of the intermetallic compound layer develop over the critical thickness and can be used for the reliability assessment of the solder joints subjected to thermal aging

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Business Perspectives on MCM, MEMS & MEOMS Packaging

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Abstract: This paper discusses business and product level considerations for multichip packaging, micro-electro-mechanical systems (MEMS) and micro-electro-optical-mechanical systems (MEOMS) as cost effective alternatives in the design and manufacture of communications systems and telephony products. Important aspects include component functionality and complexity, acquisition and logistics costs, product modularity and integration. MCMs, MEMS and MEOMS offer unique solutions and significant system level cost savings in many applications, e.g. RF modules, antennae tuning, digital matrix functions, optical switching and product options such as security, data storage, voice recognition, etc.

Introduction: Throughout the 1980s and 1990s, promotion of conventional microelectronic assembly solutions such as hybrids and multichip modules focused on performance aspects of these technologies. As the new millenium approached many began to recognize that the true value of these microelectronic assembly options lie in miniaturization and integration of specific funtional combinations into a single package.

As we move into the age of telecommunications dominance of the electronic products sector of the global economy, high volumes of complex products create greater opportunity for the application of multifunctional package alternatives, including MCMs, MEMS and MEOMS, by driving cost curves lower and lower. This builds on the growing demand for greater bandwidth, data capacity and speed expectations in the market place as well.

Key driving forces for functional integration and miniaturization as well as performance come from rapid growth in the internet as both a communication mode and a primary conduit for business exchange. For example, late in the year

2000 data traffic volume carried by the global communications network actually exceeded the volume of voice traffic for the first time.

Focus on Mobile Telephony: The variety of mobile or wireless telephony applications ranges from pagers and cellular handsets to email appliances and wireless internet tools. Each product, as well as each geographic and/or cultural market segment creates unique customer expectations.

Pagers generally present the most simple application and may frequently be integrated into essentially a single, or at most two, basic functional modules. These include the RF function and the data conversion function, which may include text messaging.

Email appliances come next in product simplicity, requiring the same basic functionality as pagers with the addition of a keyboard or stylus input function as well as RF transmission capability.

Wireless internet access functions add significant programmability and higher performance two way transmission

requirements to the product. Input and navigation functions become slightly more complex (or at least varied) in comparison to email appliances, but the limited browsing capability imposed by a portable form factor keep overall product complexity in line with the typical email specific product. Future products may need to incorporate some sort of finger print recognition capability for internet procurement applications.

Clearly the most complex and diverse module applications lie in cellular handsets where functional requirements of all the previously described applications essentially come together. The cellular handset requires two way RF capability, complex digital multiplexing, input functionality and power control such as overvoltage protection circuitry. Cell phones of the future will likely add voice control, perhaps voice recognition for security purposes, and perhaps even global positioning system (GPS) capability.

Considering the high volumes expected in these markets, the opportunity for cost effective manufacture looks good. And clearly, each of these applications demands certain price targets be met in order to create the expected product demand in the marketplace.

Module Partitioning: Prime targets for early adoption of module implementations focus on the RF functions and some of the more complex digital sub-systems, particularly in cell phone handsets.

RF modules hold special appeal due to the complexity and expense of attempts to integrate at the semiconductor level. For example, high frequency GaAs drivers for the antenna cannot be easily integrated at the chip level with the control circuitry usually designed in silicon. An additional advantage of modularizing the RF front end comes from the test ability to

fully characterize and trim the analog functions of the module prior to assembly into the handset itself. And further, the ability to incorporate dual band, or even triple band transceiver capability into a module enhances product market applicability (See Figure 1.). This generally results in significantly higher final product assembly yield and thereby reduced trouble shooting and rework expense.

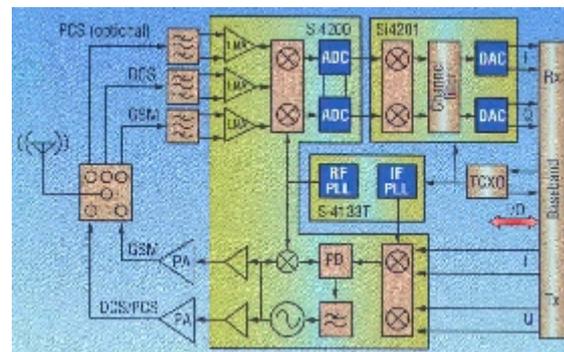


Figure 1. Three chip triple band GSM transceiver module block diagram (Silicon Technologies).

The relatively high complexity of the digital partition in a cell phone creates a second module opportunity for significant reduction in the total pincount for this part of the product. A typical handset requires three (3) to five (5) separate chips to fully manage the digital functions. In miniaturized form factors this results in up to 400 or 500 input/output points on the cell phone printed wiring board (PWB). Incorporating these chips into a single module may reduce this I/O count to as little as 200 to 250 in a slightly smaller footprint. The ultimate impact? A dramatic reduction in PWB complexity and thereby cost.

As wireless internet access continues to grow in importance, both independantly and as a cellular handset option, digital functions such as personal management functions like appointment calendars, phone directories, website

URLs, etc. will create additional demands for functional integration. For purposes of internet purchases security requirement generate an expectation from customers that systems protect their identity and credit. Tools such as finger print recognition, voice printing or eye retina identification systems will find their way into both stationary and portable systems. These present additional module opportunities.

One final, yet major modularization opportunity lies in knowing the location of a device through interaction with the GPS network. This function provides major opportunity for high volume usage through recovery of lost or stolen property, coordination with mapping information to identify convenient locations for users for items such as restaurants, hotels, shortest or best traffic routes to selected destinations, etc. A GPS receiver remains somewhat complex today, but continued integration of the digital functions will soon allow design and manufacture of a simple module for easy integration into multiple application environments.

Additional module application opportunities come from the base station and routing network arena where bandwidth and capacity limitations cause mobile telephony frustration on the part of end users. Examples include vector modulators (See Figure 2.), optoelectronic repeaters, power amplifiers, etc.

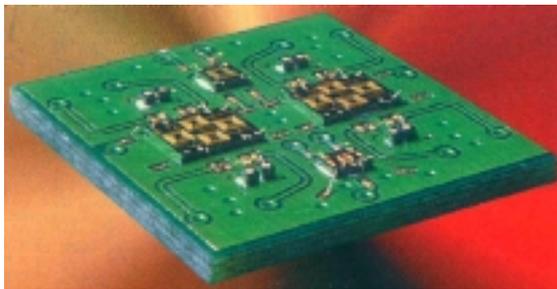


Figure 2. Eight chip base station vector modulator BGA form factor MCM (Alpha Industries).

In summary, candidates for modularization in portable products, and mobile telephony in particular, abound. RF modules, digital matrices, personal digital assistant functions, security systems, GPS location and integration, etc. can be expected to support strong growth of module designs in the foreseeable future.

Benefits of Modularization: The use of modules will soon drive even more rapid market growth in those markets that take advantage of them. Key benefits include: accelerated time to market, and more importantly, time to volume production; simplified product modularity/partitioning, engineering design changes, functional enhancement and modeling; lower cost through simplified PWB structures, higher assembly and test yields, and reduced logistics overhead; and improved product reliability.

Time to market acceleration results from removal of any need to specially design key functions into a product. Only the interface between a specific, standardized module and the rest of the product functions remains necessary. This also impacts time to volume production by removing much of the prototype trouble shooting and design problem resolution from the product introduction cycle.

Having standardized modules available for these common functions greatly simplifies the design process and allows product designers to focus their energy on tailoring their products to their customer's needs rather than on making certain that isolated product functions work properly. Engineers can also focus effort on designs capable of incorporating multiple options, completely at the discretion of the ultimate customer. And in many cases perhaps even enabling easy upgrade options that customers may

implement themselves. Finally, knowing the performance specifications and limits of each module eases the design modeling and problem resolution process by providing designers with known boundaries for each function, as opposed to having to deal with multiple individual components that do not necessarily behave in predictable way when integrated into a complete function. The module designer and producer resolves these issues before the product designer ever needs to deal with them.

Cost reduction remains the ultimate judge of the value of any design approach, and modules may positively impact cost in several ways. The most obvious impact comes at the PWB level where modules allow the highest density interconnect structures to be focused only where needed. This results in larger pitch integrated components (modules) than possible using individual integrated circuits (ICs) directly on the PWB (See

Figure 3.). These simplified PWBs cost far less and result in higher assembly yields as well. In addition, since module procurement results in essentially “know good functions,” assembly yield is further enhanced through the elimination of defective interactions between individual IC components. This also significantly improves final product reliability since most infant failures and marginal performance interactions (among components) disappear.

The final cost impact comes from the logistics arena where the simple cost to create and manage a part number in the manufacturing resource planning system at a major corporation can run into the US \$100,000 to US \$150,000 range. For a major OEM the use of a single module in a product design, as opposed to five or six individual ICs, may result in an information systems cost savings of as much as \$500,000 per year!

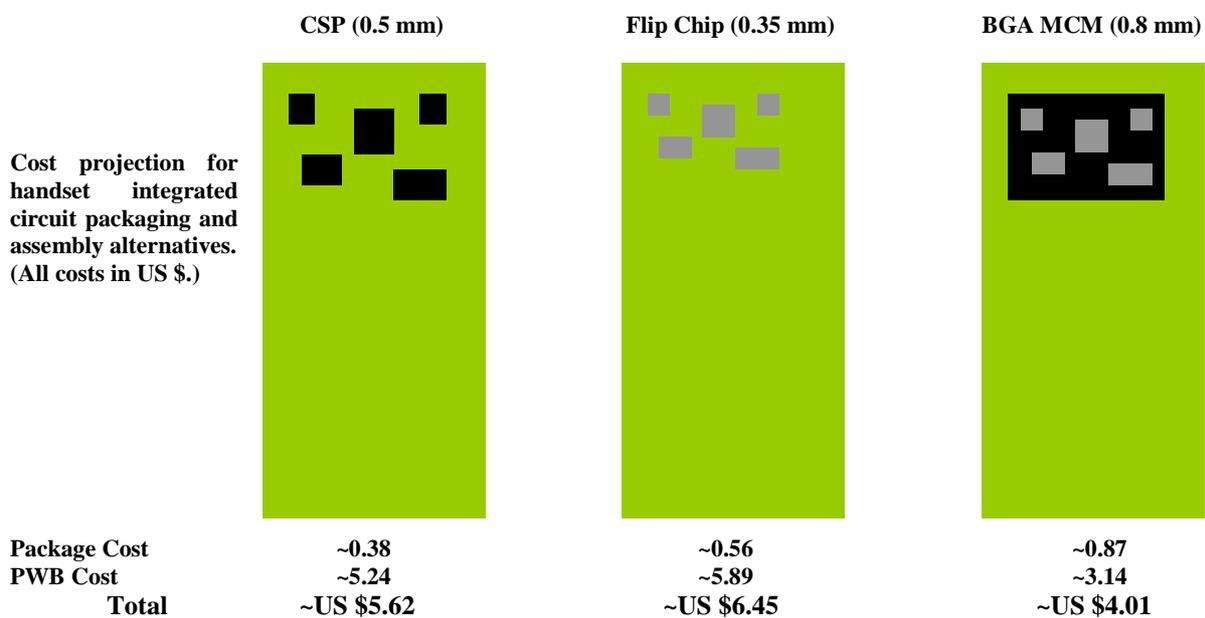


Figure 3. Potential cost savings estimate using multichip packaging versus chip scale (CSP) or flip chip alternatives.

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Recent target technology areas include MCM, MEMS and MEOMS packaging as well as opto-electronics assembly and high density substrates, both organic and inorganic. Dr. Bauer lectures throughout Asia, Europe, South America, Australia/New Zealand and the USA on these topics from both a technical and market perspective.