

## *Session FC-2*

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# Fluxless Solder Bumping in Flip Chip Package by Plasma Reflow

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## Abstract

A new fluxless reflow process using Ar+10%H<sub>2</sub> plasma was investigated for application to solder bump flip chip packaging. The 100  $\mu\text{m}$ -diameter Sn-3.5wt%Ag solder balls were bonded to 250  $\mu\text{m}$  pitch Cu/Ni under bump metallurgy (UBM) pattern by laser solder ball bumping method. Then, the Sn-Ag solder balls were reflowed in Ar+H<sub>2</sub> plasma. Without flux, the wetting between solder and UBM occurred in Ar+H<sub>2</sub> plasma. During plasma reflow, the solder bump reshaped and the crater on the top of bump disappeared. The bump shear strength increased as the Ni<sub>3</sub>Sn<sub>4</sub> intermetallic compounds formed on initial reflow stage but began to decrease as coarse (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> grew at solder/UBM interface. As the plasma reflow time increased, the fracture within solder bulk decreased and the fracture along solder/UBM interface increased. The off-centered bumps self-aligned to UBM pattern during plasma reflow. The solder ball defect occurred in high power and a long time plasma reflow.

## Introduction

The development of personal and portable electronics, such as cellular phone, laptop computer and IC card, forced the semiconductor assembly industry to meet the need of miniaturization and lightweight of the products. Accordingly, the pitch size of the semiconductor package has grown finer and finer. The solder bump flip chip technology, which is an ultimate way to increase the packaging density, is widely used for fine-pitch connection between high-I/O components and substrates. It has proven to be a high-yield and reliable joining technology. The flip chip package has extended its application to optoelectronics and MEMS(Micro Electro Mechanical System) package.[1]

The flux in soldering removes contaminants and dissolves surface oxides to improve wettability and solderability. The application of flux, however, could lead to the corrosion of the circuit and deterioration of the long-time reliability due to the flux residues in the joint which should be require cleaning after soldering.[2] Especially in fine pitch flip chip package, the residual flux may exist in the region where the inspection and removal of the residue are almost impossible. Besides, the flux cleaning solvents are proved to have detrimental effect on environment. Since using flux causes environmental concerns manufacturer needs to find an effective replacement of the flux. Therefore, fluxless flip chip soldering is becoming an active research area.

Figure 1 represents a typical solder bump structure. Solder evaporation through aligned metal mask[3], solder alloy

electroplating[4], stencil solder paste printing[5] and solder wire stud bumping[6] are main flip chip solder bumping techniques which are applied in current package industry. One of the common processes of these bumping techniques is the reflow with flux. The evaporated, plated, or printed solder on defined UBM (Under Bump Metallurgy) patterns is fluxed and reflowed. The objects of the reflow are 1) to make ball-shaped bumps 2) to get homogenous solder bump composition 3) to insure the bump height uniformity and 4) to enhance the adhesion strength to UBM.

The conventional reflow is usually processed in an oven-type or conveyor-type reflow furnace after flux is applied to the solder bumps. The temperature of the furnace increases to 30~50 °C higher than the melting point of solder. In the reflow, flux helps the balling of melted bumps by removing surface oxide as well as reducing the surface tension.

The purpose of this study is to develop a new reflow process using Ar+H<sub>2</sub> plasma instead of flux. Plasma treatment using the energetic particle from a glow discharge is one of the alternative methods to the application of flux. As a dry cleaning process, plasma treatment produces little or no waste byproducts, and is therefore far more attractive than solvent or acid based techniques where gallons of waste may be generated. The plasma treatment in soldering process is expected to eliminate the environmental concerns associated with solvent cleaning, flux and flux application system.[7]

This paper reports the application of Ar+H<sub>2</sub> plasma to fabricate Sn-3.5wt%Ag solder bump flip chip with the bump diameter of 100  $\mu\text{m}$  and pitch size of 250  $\mu\text{m}$ . Laser ball bumping method[8] was used to bond solder balls to defined UBM. The solder bump shape, bump shear strength, self-alignment and wetting to UBM will be discussed according to plasma processing parameters.

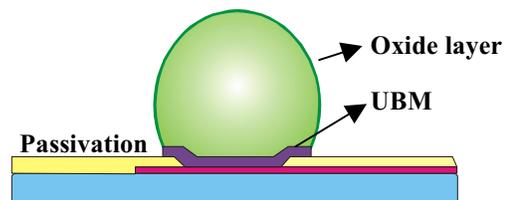


Figure 1. A typical solder bump structure in flip chip package.

## Experimental Procedure

In this work, a real semiconductor chip in production line was not used. Instead, a test chip using Si-wafer as the substrate was fabricated. Firstly, Cr/Cu plating seed layer was

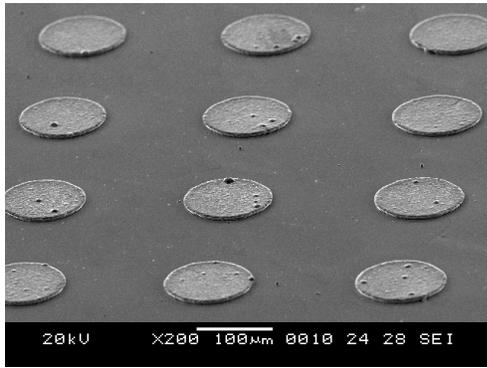


Figure 2. The 250  $\mu\text{m}$  pitch Cu/Ni UBM pattern electroplated on Si-wafer. The diameter of the pad is 100  $\mu\text{m}$ .

deposited on Si-wafer. Through 9  $\mu\text{m}$ -thick positive PR (photo resist) photolithography, the mold for UBM electroplating was made. Then, 4  $\mu\text{m}$ -Cu and 4  $\mu\text{m}$ -Ni UBM layers were plated sequentially to the Si-wafer at the current density of 10mA/cm<sup>2</sup>. After UBM plating, PR mold and seed layer were removed to form the 100  $\mu\text{m}$  diameter of Cu/Ni UBM pattern on Si-wafer as in figure 2.

Sn-3.5wt%Ag solder balls of 100  $\mu\text{m}$  diameter were bonded to the UBM pattern by laser solder ball bumping process. A solder ball was singulated and placed on UBM by capillary. Then, the solder ball was radiated by the Nd:YAG laser with the wave length of 1064nm with laser current of 65A and laser pulse width of 3ms. The solder ball was bonded to UBM and the shear strength right after bonding was about 3~6gram-force.

After the initial bonding by laser, the solder ball was reflowed in low temperature RF Ar+H<sub>2</sub> plasma. The plasma gas consisted of 90vol.%Ar and 10vol.%H<sub>2</sub> gas. The pressure of chamber was kept 270torr during plasma reflow. The RF power of plasma was set to 100W and 200W. The reflow time range was 0~120 seconds. Another initially bonded bump specimen was fluxed and reflowed on hotplate at 250°C for 0~120 seconds. The VOC-free flux (SF-531, Soltec.) was used.

The bump adhesion strength was estimated with micro-shear tester (Rhesca PTR-1000) for solder bumps reflowed by plasma and flux. The stylus of the tester was set 5  $\mu\text{m}$  higher than UBM thickness and the moving speed was 200  $\mu\text{m}/\text{s}$ . The shear strength's of bumps reflowed by plasma and flux were compared.

The bump shape after reflow and the fracture surface after shear test were examined with SEM. After plasma reflow, the solder bump was selectively etched by Nitric acid and the remained intermetallic compounds were analyzed by SEM and EDS.

## Results and Discussion

Figure 3 shows the shape of Sn- 3.5Ag solder bumps reflowed in different conditions. The shape of the bump right after the laser bonding at 65A, 3ms condition is given in figure

3(a). The abrupt local laser radiation made the ball bonded partially with the UBM somewhat mis-aligned from the center.

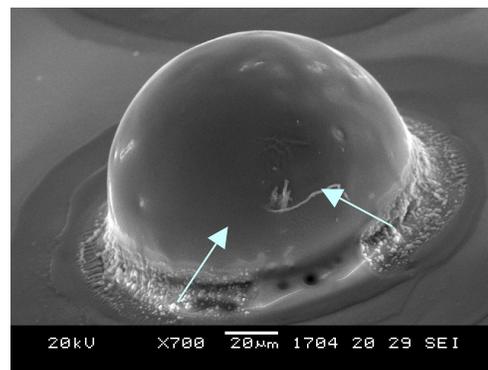
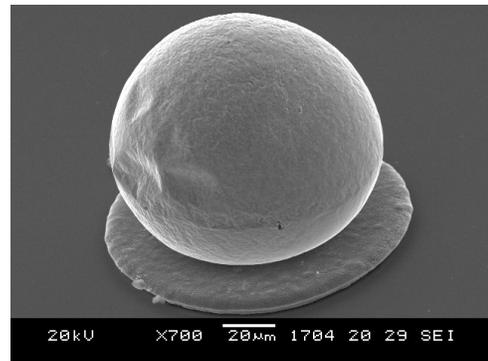
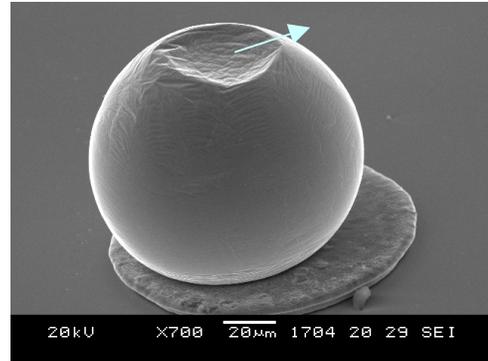


Figure 3. Sn-3.5wt% solder bump shape reflowed in different condition. (a) as-bonded solder ball by laser 65A, 3ms. (b) reflowed on hotplate at 250°C for 60s without flux. (c) reflowed on hotplate at 250°C for 60s with flux.

The joint between solder ball and UBM had sharp notch at which stress may be concentrated in shear loading.

On top of the bump, there was a crater originated from rapid cooling. The crater may be a cause of void at flip chip solder joint if gas is trapped in. The crater will not appear if the laser current or pulse width increases. However, at high current or long pulse width condition, the frequency of capillary clogging also increases, so that the life of the capillary may be reduced. Therefore, reflow of the ball is required after initial bonding at low laser current to reshape the bump and to increase adhesion strength with UBM.

Figure 3(b) represents the bump shape after reflow of the laser bonded bump on hot plate at 250 °C for 60s without flux in air. The volume expansion by melting removed the crater on top of the bump. However, the melt was confined in the oxide layer on solder surface like the water in plastic bag. So, the wetting with UBM occurred little. Also, the sharp notch at the joint still existed.

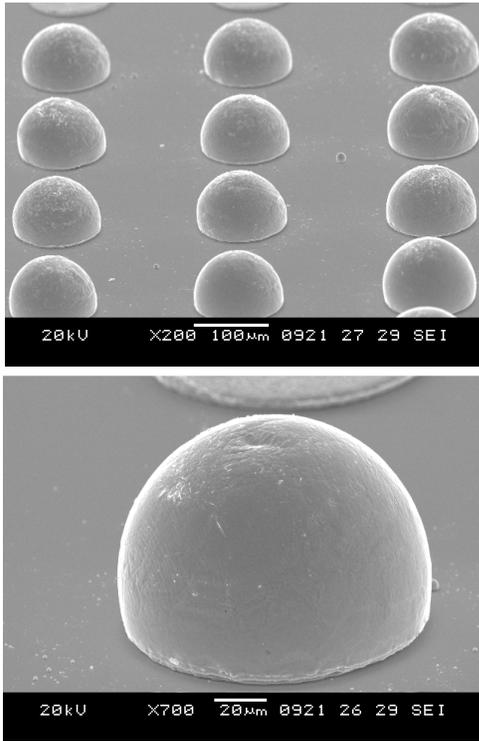


Figure 4. Sn-3.5wt%Ag solder bump reflowed in Ar+10% $H_2$  plasma at 100W for 60s.

The shape of the bump reflowed on hot plate at 250 °C for 60s with flux is shown in figure 3(c). As was expected, the bump was reshaped, so that the crater disappeared. The solder wetted the UBM and the notch at the joint also disappeared. However, there were flux residues around the solder bump, so adequate flux cleaning was required. The residual flux may affect the reliability of the flip chip package due to the negative effect on underfill materials.[9] In case of optoelectronic device package, the laser signal may be deflected or attenuated by flux residues and impact the performance of the components.[10] Therefore, the demand for fluxless reflow will increase as the bump pitch gets finer.

Figure 4(a) shows 100  $\mu m$  Sn-3.5Ag solder bump pattern with 250  $\mu m$  pitch size after reflow in Ar+10% $H_2$  plasma at 100W for 60s. Figure 4(b) shows that the crater disappeared by bump reshaping and the solder wetted the UBM. Therefore, it is evident that the fluxless reflow using Ar+ $H_2$  plasma is quite effective.

Figure 5 shows the top view of Sn-Ag solder bump reflowed in Ar+ $H_2$  plasma at 100W for 0~120s. The off-centered solder ball about 30  $\mu m$  from UBM began to reshape

at 40s (figure 5(b)) and completely self-aligned to the UBM pad at 60s. (figure 5(c)) The shape of the bump reflowed in the plasma for 120s (figure 5(d)) changed little but small solder balls with the size of 1~5  $\mu m$  were spattered around the bump.

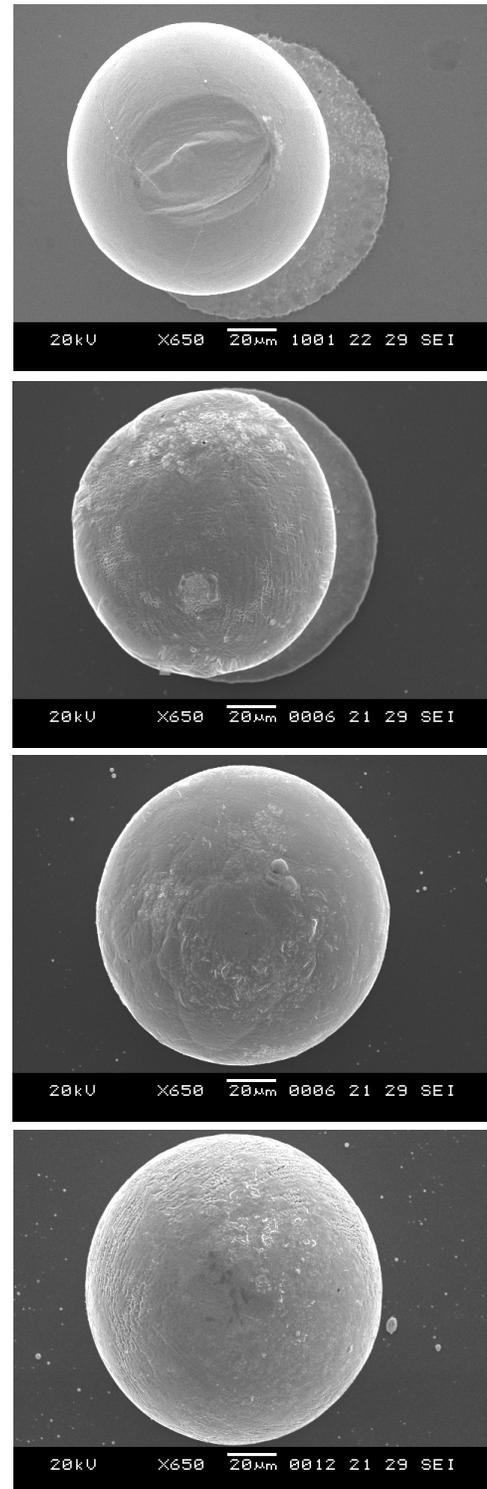


Figure 5 Top view of Sn-3.5wt%Ag solder bump reflowed in Ar+10% $H_2$  plasma at 100W. (a) 20s (b) 40s (c) 60s (d) 120s

Figure 6 shows variation of bump shear strength with plasma reflow time at different plasma power. At plasma power of 100W, the shear strength did not increase by 20s but began to increase rapidly at 30s. The shear strength reached maximum 85gram-force after 100s and decreases thereafter. At power of 200W, the strength increased after 10s, reached maximum strength at 20s, and decreased after. The shear strength of the bump reflowed on 250°C hot plate with flux is also plotted in figure 6. The strength was kept 60~80gram-force to the reflow time of 120s.

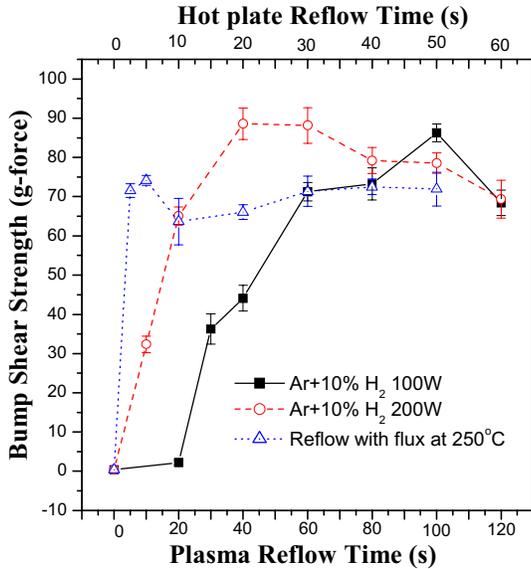


Figure 6. Sn-3.5wt% solder bump shear strength on Cu/Ni UBM with different reflow condition.

Figure 7 represents the fracture surface of plasma-reflowed solder bump at 100W power after shear test. The laser bumped solder ball was partially bonded to UBM as seen in figure 7(a). The solder bump reflowed in Ar+H<sub>2</sub> plasma for 40 and 60s fractured within solder bulk for the most part but minor part along solder/UBM interface at the end of shearing. The fracture surface of solder bump reflowed for 120s was mainly along solder/UBM interface. That is, as the plasma reflow time increases, the fracture surface changes from within solder bulk to along solder/UBM interface.

The top view of the intermetallic compound (IMC) at the interface between solder and UBM is displayed according to reflow time at 100W power in figure 8. The IMC was identified by EDS analysis. The Ni<sub>3</sub>Sn and Ni<sub>3</sub>Sn<sub>4</sub> IMC's were observed in the bump reflowed for 20s. In the 40s specimen, coarser Ni<sub>3</sub>Sn<sub>4</sub> IMC was observed and in 60s specimen, plate-type (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> IMC formed. In the solder/UBM interface reflowed for 120s in Ar+H<sub>2</sub> plasma, only coarsely grown (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> IMC was observed. It seemed that during plasma reflow, the bump shear strength increased as the Ni<sub>3</sub>Sn<sub>4</sub> IMC formed on initial reflow stage but began to decrease as coarse (Cu,Ni)<sub>6</sub>Sn<sub>5</sub> formed at the interface after 60s. In case of plasma reflow at 200W, heating seemed to be more severe so

that the shear strength reached maximum value more earlier than in case of 100W-reflow.

The mechanism of Ar+H<sub>2</sub> plasam reflow is suggested in figure 9. As-bumped solder ball by laser is locally bonded with UBM and surrounded by oxide layer with a crater on top of it as in figure 9(a).

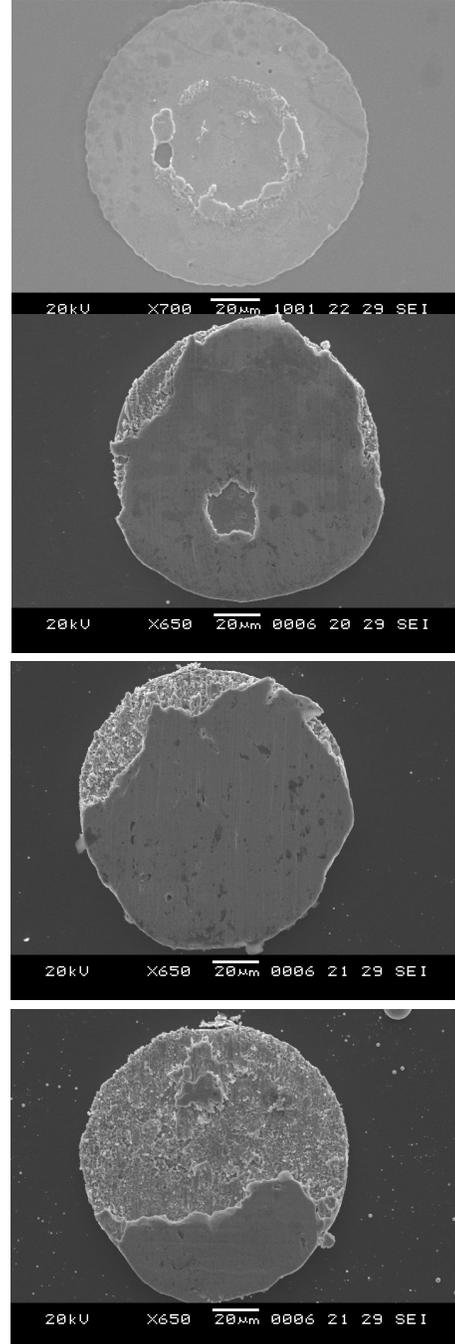


Figure. 7. Fracture surface of Sn-3.5wt%Ag solder bump reflowed in Ar+10%H<sub>2</sub> plasma at 100W. (a) 0s (b) 40s (c) 60s (d) 120s

When the ball is reflowed in Ar+H<sub>2</sub> plasma, the oxide layer on solder and UBM surface is broken by Ar<sup>+</sup> ion

bombardment. The momentum energy of  $\text{Ar}^+$  ion is transferred to heat energy by collision to solder bump and the solder is heated to melting point. (figure 9(b)) The reducing atmosphere of  $\text{H}_2$  plasma prevents molten solder from re-oxidation. The reshaping and self-alignment begins by surface tension of liquid solder. (figure 9(c)) The molten solder reacted with the UBM and IMC formed. (figure 9(d))

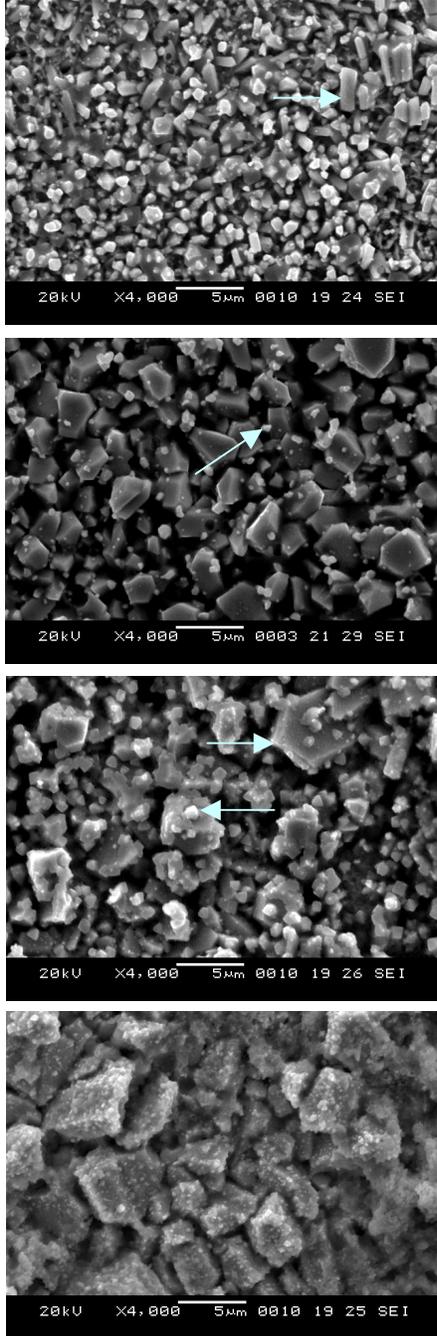


Figure 8. Top view of intermetallic compound at the Sn-3.5wt%Ag solder/UBM interface reflowed in  $\text{Ar}+10\%\text{H}_2$  plasma at 100W. (a) 20s (b) 40s (c) 60s (d) 120s

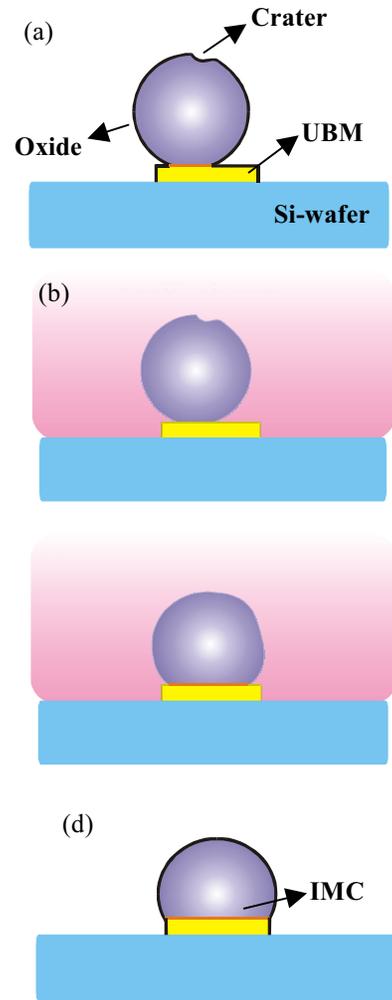


Figure 9. Mechanism of  $\text{Ar}+\text{H}_2$  plasma reflow.

(a) As-bonded solder ball by laser.

(b) Oxide layer is removed by  $\text{Ar}^+$  ion bombardment. Solder is melted by plasma heat.

(c) Reshaping and self-alignment begins by liquid surface tension.

(d) Molten solder reacted with UBM and IMC formed.

Figure 10 shows Sn-3.5Ag solder bump reflowed in 200W-plasma for 40s. Very small solder balls are distributed around the bump with the size of  $1\sim 10\ \mu\text{m}$ . The defect "solder ball" is known to form when the heating rate is fast. [11] In this work, the solder ball was found after 60s at 100W power and after 20s at 200W power. The solder ball may be a cause of short

circuit in the finer pitch flip chip package. Therefore, the plasma power and reflow time must be controlled lest the solder ball occur.

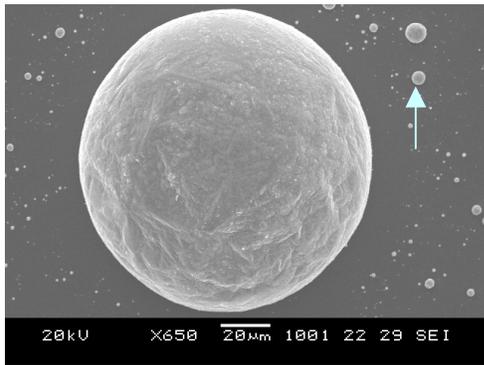


Figure 10. Solder balls distributed around Sn-3.5wt%Ag solder reflowed in Ar+10%H<sub>2</sub> plasma at 200W for 40s.

Although the plasma reflow was applied to the laser-bonded solder ball in this study, it will be possible to apply to other solder bumping technologies, such as evaporation, electroplating, stencil printing, and solder wire stud bumping etc.

### Conclusions

A fluxless reflow method using Ar+10%H<sub>2</sub> plasma was studied and applied to Sn-3.5wt%Ag flip chip solder bump. The plasma reflow was very effective for ball shaping. As the wetting between solder and UBM began, bump shear strength increased. During plasma reflow, the self-alignment of off-centered bumps occurred during plasma reflow. Sputtering action of Ar plasma, reducing atmosphere of H<sub>2</sub> plasma and plasma heat energy seem to be the main factors for plasma reflow. The solder ball defect occurred in excessive plasma reflow. If the plasma power can be controlled as the temperature profile of conventional reflow, the plasma reflow will be able to applied to optoelectronics and MEMS package where the use of flux is restricted.

### Acknowledgements

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# A Thermode Bonding Process for Fine Pitch Flip Chip Applications Down to 40 Micron

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## Abstract

As the density of electronic packaging continues to increase interconnection technologies for finer pitches down to 40 micron are required. Solder joining is still the most common technology for flip chip assemblies. Stencil printing is appropriate down to pitches of 200 micron to create solder balls. For finer pitches smaller solder volumes and new assembly processes are needed. In this paper a cost effective maskless bumping technique to create thin solder caps and a fast thermode bonding process are presented. For the thermode bonding process in a first step noflow underfiller is applied on the substrate e.g. by stencil printing. Using a flipchip-bonder the chip is soldered on the substrate by fast heating of the tool and low pressures. This work is focused on the assembling process of flip chips with pitches down to 40 micron on different substrate types like silicon and flexible substrates. The effect of the small gap due to the thin solder caps and the increased influence of the formation of intermetallic compounds are studied. Results of reliability investigations such as thermal cycling and temperature humidity testing are shown.

## 1 Introduction

Due to the requirements of new mobile, light, small and multifunctional electronic products the increasing density of the IC's lead to a larger number of I/O's at the same footprint area of the chip. So flip chip technology becomes more and more attractive as wire bonding is a sequential interconnection technique. Soldering is still the most common technology for flip chip assemblies. Typically stencil printing of solder paste is used to create solder balls for pitches down to 200 micron [1;2]. In flip chip technology the chip with solder balls is placed face down on the substrate and reflowed. Underfilling of the soldered IC is necessary to achieve high reliability. The use of no-flow underfiller for a concurrent underfilling and solder joining processes has been invented and developed in the last few years [3;4;5].

For smaller pitches than 200 micron normal printed solder balls will lead to solder bridges between adjacent contacts during reflow process. To prevent this a new bumping technology to create smaller solder volumes on the bond pads has been developed [6;7;8;9]. This immersion solder bumping

technology is suitable to make solder caps on bond pads down to 40 micron.

Due to the thin solder caps new assembling technologies have to be developed. In this paper a thermode bonding technique in combination with the use of no-flow underfiller is shown.

## 2 Technologies

### Bumping technology

For low-cost wafer bumping stencil printing of solder paste was implemented and has gained a high interest for flip chip soldering. A large variety of solder pastes including lead-free alloys are available. However due to available solder pastes and stencil geometries this process is limited in pitch down to 200  $\mu\text{m}$  for high volumes and 150  $\mu\text{m}$  for special layouts and laboratory scale experiments.

For very fine pitches down to 40  $\mu\text{m}$  immersion solder bumping (ISB) can be a low-cost alternative compared to electroplating. First electroless Ni/Au is used as UBM. Then the wafer is immersed in liquid solder as shown in figure 1. The Ni UBM is wetted and a small solder cap is formed on top of Ni.

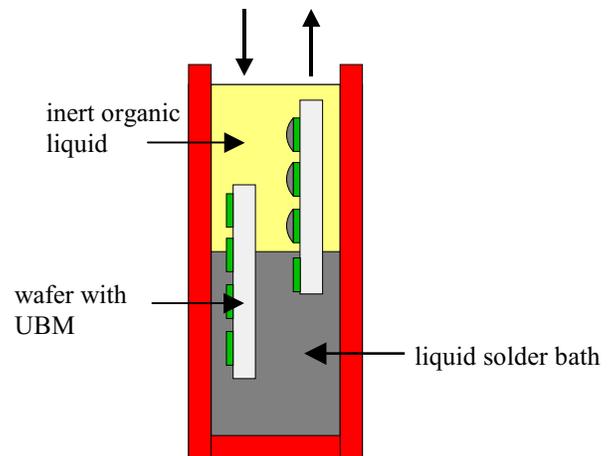


Figure 1: Principle of immersion solder bumping

An organic liquid prevents oxidation of solder and improves wettability. After soldering, residues can be easily

removed. The process is available for wafers with different sizes up to 6 inch.

Figure 2 gives an overview of 5  $\mu\text{m}$  Ni/Au bumps immersed with eutectic PbSn solder at 50  $\mu\text{m}$  pitch. The solder cap height strongly depends on the pad size, Ni bump height and solder material. The average solder cap height at 100  $\mu\text{m}$  pitch (pad diameter 50  $\mu\text{m}$ ) is 8  $\mu\text{m}$ , at 40  $\mu\text{m}$  pitch (pad diameter 20  $\mu\text{m}$ ) there is only about 3  $\mu\text{m}$  solder on top of the Ni-UBM.

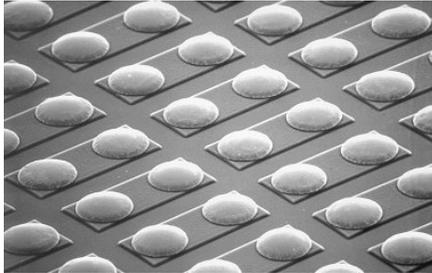


Figure 2: Overview of immersed Ni/Au bumps at 50  $\mu\text{m}$  pitch

Normal flip chip assembly using reflow processes is not suitable for those small solder volumes with the typical large deviation. In addition the gap height is reduced so that the flow of normal underfiller will lead to very long cycle times if it is possible at all. To prevent these problems the preapplication of “noflow” underfiller using either stencil printing or dispensing followed by a thermode bonding process including placing and soldering are investigated.

#### Thermode bonding technology

Thermode bonding processes using pulse heated thermodes were described in different works before. In figure 3 the packaging process using “noflow” underfiller and a thermode bonder is shown.

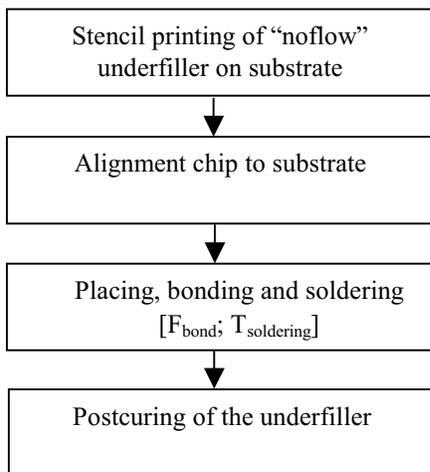


Figure 3: Packaging process flow

For the present investigations a Flip Chip Bonder FC150 from Karl Sues was used. This bonder is a full automatic high

accuracy flip chip bonding machine and can reach heating rates of about 20  $\text{Ks}^{-1}$ . The formerly used modified TAB bonder can not achieve the high accuracy needed for the assembling of chips at 40  $\mu\text{m}$  pitch. The chuck of the FC150 is shown in figure 4.



Figure 4: Chuck view of the FC150 bonder

In a first step the “noflow” underfiller has to be applied on the substrate. Therefore a manual stencil printing method was used. In order to prevent a contamination of the bonding tool during the thermode bonding process it is necessary to achieve a good volume control of the applied amount of underfiller. In figure 5 the simple printing method is depicted.

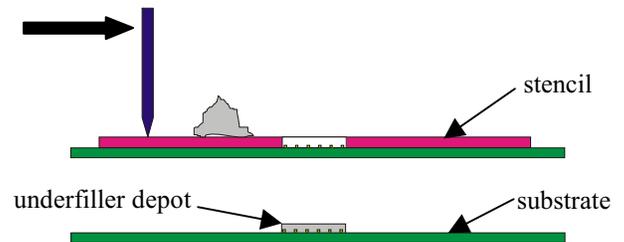


Figure 5: Printing of “noflow” underfiller

As the underfiller only starts to cure during the bonding and soldering process a post curing of the package has to be done.

### 3 Test vehicles (TV)

To investigate the influence of small solder volumes on the reliability of flip chip assemblies different testchips and substrates were used. This work was focused on 100  $\mu\text{m}$  pitch testchips on flexible substrates (TV1) with and without copper stiffener and on 100  $\mu\text{m}$  pitch testchips on Silicon substrates (TV2). Besides the testvehicles at 100  $\mu\text{m}$  pitch first samples of TV2 (Si on Si) at 40  $\mu\text{m}$  pitch were assembled.

All Si-testchips were bumped with eutectic PbSn67 solder using the immersion solder bumping technology. The flexible substrates were metallized with Cu/Ni/Au, without soldermask. The final metallization of the Si-substrates was Ni/Au.

For electrical characterization of the soldered contacts on TV1 a Daisy-Chain and 8 Four-Point-Kelvin structures were designed.

TV2 at 100  $\mu\text{m}$  pitch has only a Daisy-Chain. The following table 1 gives an overview of the used testvehicles and measurements.

	chip	# of bumps	substrate	measurements
TV1 100 $\mu\text{m}$ pitch	Si 25 $\text{mm}^2$	176 peripheral	flexible	DC 8 FPK
TV1 100 $\mu\text{m}$ pitch	Si 25 $\text{mm}^2$	176 peripheral	flexible with stiffener	DC 8 FPK
TV2 100 $\mu\text{m}$ pitch	Si 1,94 $\text{mm}^2$	95 area array	Si	DC
TV2 40 $\mu\text{m}$ pitch	Si 0,96 $\text{mm}^2$	90 area array	Si	no

Table 1: Specification of the testvehicles

### 3 Experimental

#### Properties of used "noflow" underfiller

A commercially available noflow underfiller was selected for the present work. The material properties are listed in table 2 below.

Properties	Unit	
CTE $\alpha_1$ ( $T < T_g$ )	ppm/K	76
CTE $\alpha_2$ ( $T > T_g$ )	ppm/K	202
$T_g$	$^{\circ}\text{C}$	124
Young's Modulus@50 $^{\circ}\text{C}$	GPa	2

Table 2: Material properties of used underfiller

In former investigations [3] this material has shown very good reliability results and no problems regarding voids in the underfilled packages. It is an unfilled, high  $T_g$  material with good viscosity properties for application using stencil printing. After the thermode bonding process a post curing of 30 min at 150 $^{\circ}\text{C}$  is necessary.

#### Thermode bonding process specifications at FC bonder FC150

In figure 3 the most important steps for the thermode bonding process using "noflow" underfiller were shown. As the solder volume of each bump is very small the problem of solder bridges between adjacent contacts is minimized. Therefore it was possible to work with the more easy force control instead of the height control. During the soldering process the oxidized surface of the immersion solder bumps has to be cracked. Therefore a bonding force of 40 N soldering a 25  $\text{mm}^2$  chip containing 176 bumps at 100  $\mu\text{m}$  pitch was applied as an optimum.

The bonding temperature depends on the used solder and has to be about 40 K higher than the melting point. In order to reduce the phase formation between substrate metallization, UBM and solder the soldering time has to be as short as possible. On the other hand the underfiller has to start gelling to tack the chip onto the substrate surface during the soldering process. This is necessary because of the lower mechanical

stability of these small and thin soldered contacts in comparison to conventional reflowed soldered bumps.

In general there is no difference in the temperature profile for the different testvehicles as always the same solder was used. Regarding the number and size of the bumps the bonding force has to be reduced to 10 N for assembling process of TV2. In figure 6 and 7 the temperature and bonding force profiles used at the FC150 for the thermode bonding process at 100  $\mu\text{m}$  pitch are depicted.

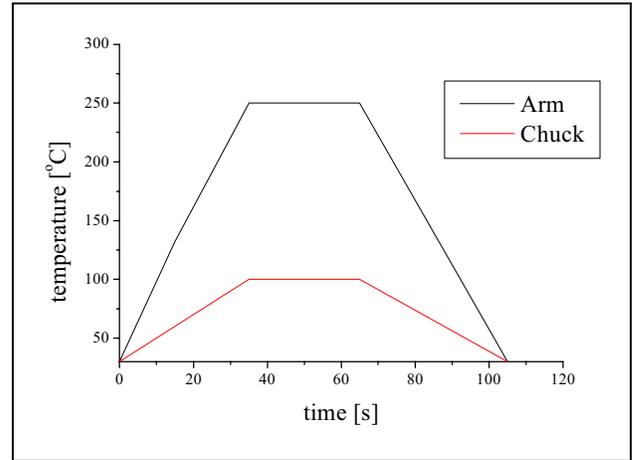


Figure 6: Temperature profiles for thermode bonding process at 100  $\mu\text{m}$  pitch

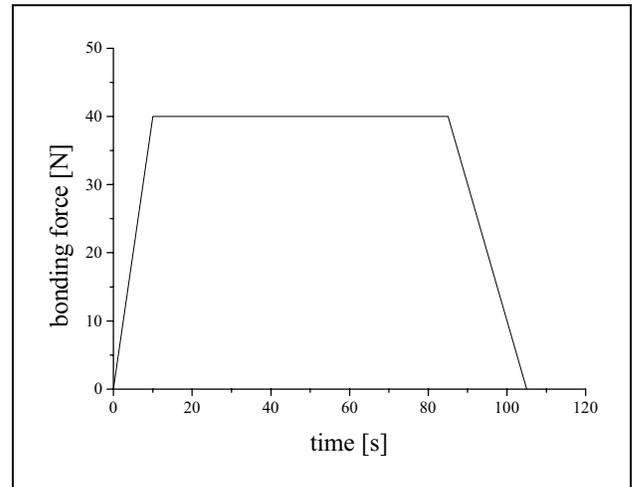


Figure 7: Bonding force profile for thermode bonding process at 100  $\mu\text{m}$  pitch

#### Initial state after thermode bonding process

The samples at 100  $\mu\text{m}$  pitch were electrically measured after the thermode bonding process and after the postcuring. There were no differences in the measured resistances due to the total curing of the underfiller.

The first samples of each testvehicle were cross sectioned to control the shape and quality of the soldered contacts. Figure 8 shows a typical soldered contact at 100  $\mu\text{m}$  pitch TV1.

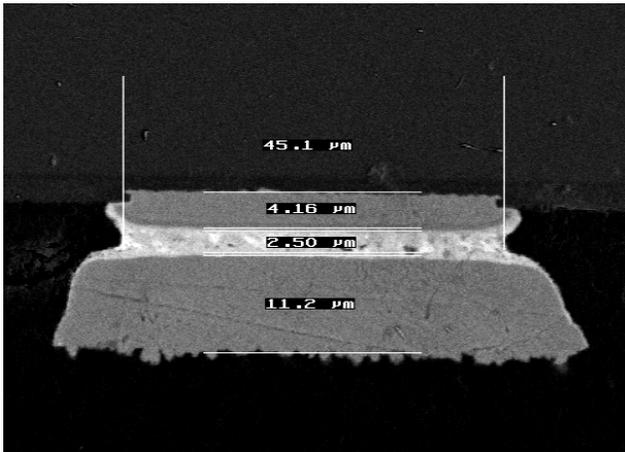


Figure 8: SEM picture of a soldered contact of TV1 in initial state (magnification 1500)

The thickness of the solder is 2,5  $\mu\text{m}$ , the diameter of the bump is around 45  $\mu\text{m}$ . The often used X-ray-examination of soldered contacts could not be used for this work because the achievable contrast in the X-ray-pictures was insufficient. This results from the very small solder volume respectively the low amount of lead.

#### 4 Reliability tests and Discussion

The fact that after the thermode bonding process the solder thickness was only 2,5  $\mu\text{m}$  leads to the assumption that intermetallic phase formation will rapidly reduce the reliability. Flip chip assemblies of testvehicle 1 with and without copper stiffener on the backside of the flexible substrate have been subjected to thermal cycling conditions. The profile was in the temperature range between  $-55^{\circ}\text{C}$  and  $+125^{\circ}\text{C}$  using a three chamber oven (10min @  $125^{\circ}\text{C}$ ; 5min @  $25^{\circ}\text{C}$ , 10min @  $-55^{\circ}\text{C}$  and again 5min @  $25^{\circ}\text{C}$ ).

Testvehicles 2 (Si on Si) at 100  $\mu\text{m}$  pitch have been put into thermal cycling as well as in temperature / humidity testing conditions at  $85^{\circ}\text{C} / 85\% \text{ r.h.}$

Electrical measurements have been taken after every 100 temperature cycles respectively 100 hours. On TV1 the DC and the 4PK-structures, on TV2 at 100  $\mu\text{m}$  pitch the DC was measured. For electrical measurements a half automatic waferprober from Karl Suess was used.

#### Reliability results of TV1

It was observed that most of the assemblies of TV1 on stiffened substrates failed after the first 100 cycles.

Flip chip assemblies bonded on not stiffened substrates showed very good reliability results during thermal cycling until 2000 cycles. Figure 9 shows the change in electrical resistivity of the mean value of the 8 measured 4PK-structures and the daisy-chain values until 2000 temperature cycles.

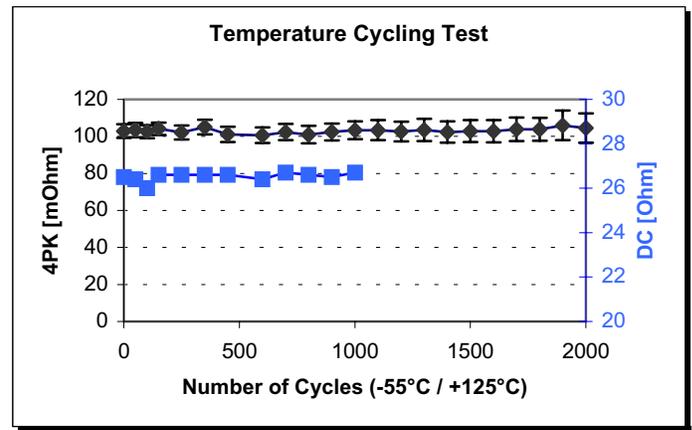


Figure 9: Change of electrical resistance of 4PK and DC during thermal cycling of TV1 without stiffener

It can clearly be seen that the daisy chain failed after 1000 cycles but the 4PK-structures are still in the range of the initial measured resistances. Also the deviation of the values of all 4PK-structures is small.

In figure 10 all measured 4PK values are depicted individually to clarify the very slow increase. The first failed 4PK-structure was detected after 1900 cycles.

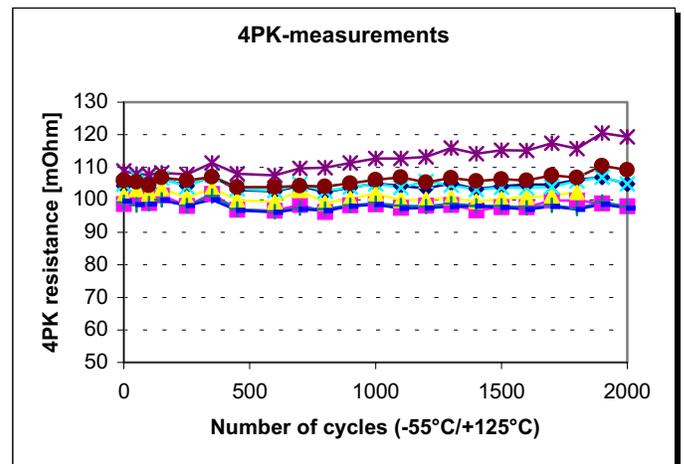


Figure 10: Measurements of 4PK-structures on TV1 without stiffener until 2000 thermal cycles

The reliability results of TV1 without copper stiffener are much better compared to those with stiffener on the substrate backside. That could be explained with the following thesis: due to the different coefficients of thermal expansions of Silicon testchips and flexible substrates during thermal cycling all mechanical stress has to be incorporated in the solder joints. Conventional flip chip solder joints of 100  $\mu\text{m}$  diameter can be loaded with stress caused from thermal cycling as they can deform themselves to spread the stress.

The very thin and small solder amounts from immersion solder bumping can't deform in that way. So the mechanical deformation through CTE's mismatch is not compensated within the solder joints and can only be incorporated by the flexible substrate. In the present investigations the required

flexibility of the stiffened substrates was not high enough. The much better behaviour of thinner substrates was similarly reported by Tie Wang [5].

Cross sectioning of TV1 assemblies has been done after 1000 and 2000 cycles to investigate failure mechanisms and formation of intermetallics.

*Reliability results of TV2 at 100 μm pitch*

The influence of thermal mismatch effects is reduced or eliminated by using Si-testchips on Si-substrates. Figures 11 and 12 show the first results of electrical measurements during thermal cycling and temperature / humidity testing. It can be seen that there is no significant change in DC resistance until 600 cycles respectively 500 hours.

Cross sectioning has been performed in order to inspect the quality of the soldered contacts.

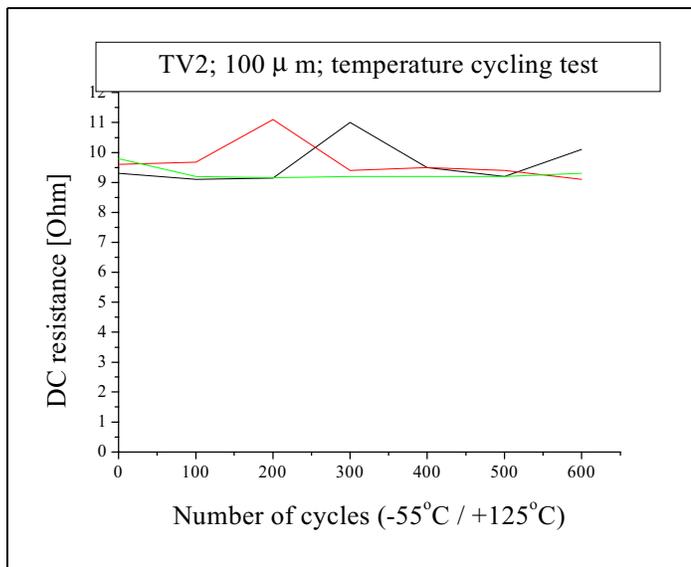


Figure 11: Behaviour of TV2 at 100 μm pitch during thermal cycling tests

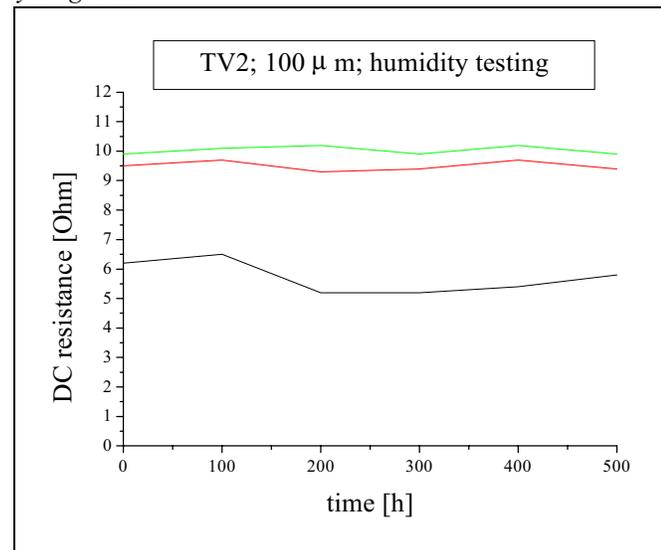


Figure 12: Behaviour of TV2 at 100 μm pitch during humidity testing

**5 Metallurgical Analysis and Discussion**

In the present case of very thin contacts of about 2.5 μm solder the metallographic preparation of cross sections is more critical in comparison to conventional bump heights of around 100 μm. Washing out of weak structural constituents such as lead-rich intermetallic phases by polishing of cross sections may falsify proper results. To prevent this, very careful grinding and polishing is required.

Investigation of formation of intermetallics seems also to be critical as most of the tin content of the eutectic solder even in initial state is used to create the metallic contact between UBM (chip side) and conductor lines (substrate side) by formation of thin Ni-Sn-phases.

Figures 13a and b show details of a cross section made from TV1 after 1000 temperature cycles.

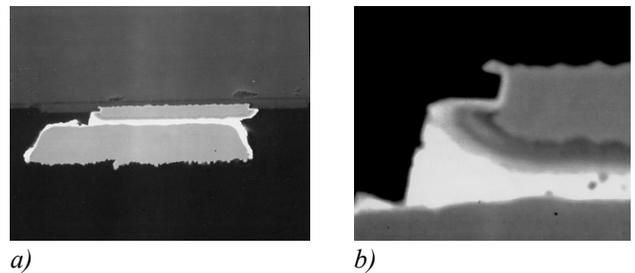


Figure 13a: SEM picture of cross section of TV1 after 1000 cycles (magnification 1000) and 13b: detail of 13a (magnification 5000)

These pictures in BSE-mode clarify the above mentioned problems in microscopic investigation methods for very small solder volumes. Most of the remaining solder component is lead. Figure 14 shows a detail of a cross section made from TV1 after 2000 cycles. There is no visible difference by comparing Figures 13 and 14.

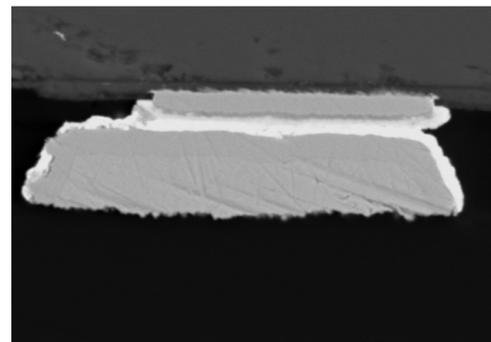


Figure 14: SEM picture of cross section of TV1 after 2000 cycles (magnification 1600)

Cross sections made of TV2 at 100 μm pitch after thermal cycling or humidity testing do not show a continuous solder layer. Figure 15 gives an example of TV2 after 600 cycles. The surface of the solder is rough, voids are visible between the UBM of the chip and substrate. Nevertheless the electrical measurements did not show a degradation in resistance.

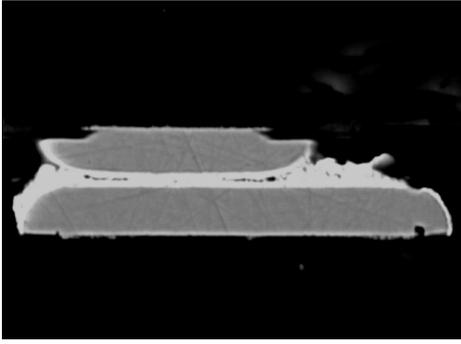


Figure 15: SEM picture of TV2 at 100  $\mu\text{m}$  pitch after 600 cycles (magnification 2000)

The voids in the solder layer may result from embedding of underfiller during thermode soldering process. This could be introduced by the surface quality of the immersion solder bumps. In general the surface is rougher than those of stencil printed solder balls.

### 6 Thermode bonding of TV2 at 40 $\mu\text{m}$ pitch

The described process for bonding of different TV at 100  $\mu\text{m}$  pitch is also appropriate for pitches down to 40  $\mu\text{m}$ . The solder cap height on the immersion soldered bump chips at 40  $\mu\text{m}$  pitch is in the range of about 4  $\mu\text{m}$ . As the chip size is reduced to 0,96 mm<sup>2</sup> more attention in application of “noflow” underfiller is important to solve the bonding tool from contaminations or even the glueing of the chip onto the heated tool.

Cross sections shown in figures 16 and 17 present an overview and a single soldered contact at 40  $\mu\text{m}$  pitch.

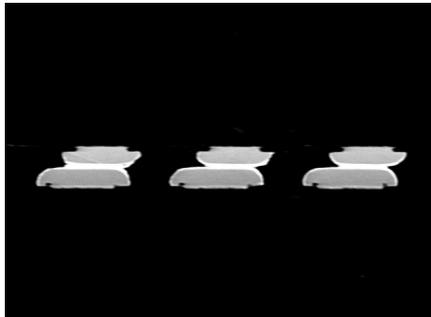


Figure 16: Cross section of a thermode bonded chip at 40  $\mu\text{m}$  pitch (magnification 1000)

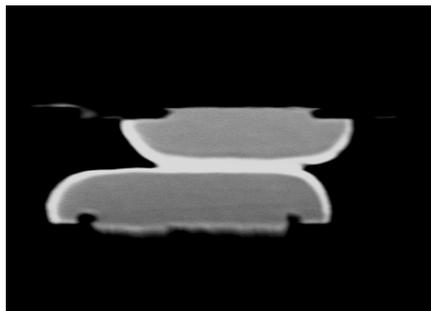


Figure 17: Cross section of a thermode bonded contact at 40  $\mu\text{m}$  pitch (magnification 3000)

Only in the direct contact area (12  $\mu\text{m}$  in diameter) between chip and substrate solder remained with a thickness of 2  $\mu\text{m}$ . In those very small dimensions it is not possible to characterize soldering quality or wettability.

### 7 Conclusions

A thermode bonding process with use of “noflow” underfiller for concurrent solder joining and underfilling has been demonstrated. Testchips were bumped using immersion solder bumping technology to create thin solder caps. Reliability tests of testvehicles at 100  $\mu\text{m}$  pitch showed good results in thermal cycling and humidity testing. Flexible and thin substrates can better dissipate stress that would otherwise be accumulated in the soldered contacts.

For fine pitch flip chip applications at 40  $\mu\text{m}$  pitch thermode bonding is suitable too. Reliability tests with different substrate types have to be done in the future to qualify this process with respect to the ultra thin solder caps.

Preapplying of “noflow” underfiller with respect to a careful volume control has been done by stencil printing. New developed spin coatable wafer level underfiller have to be tested in order to reduce production cycle times.

Faster thermode heating profiles would improve the quality of the soldered contacts concerning the remaining volume of eutectic solder. The use of lead free solder is an important topic for further investigations.

### 8 Acknowledgements

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The authors would like to thank Bettina Otto and Fabienne Jaulneau for electrical measurements.

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9. Patent Nr. DE 44 32 774 C, "Verfahren zur Herstellung meniskusförmiger Lotbumps"

# Intermetallic Formation in the Sn-Ag Solder Joints between Au Stud Bumps and Cu Pads and Its Effect on the Chip Shear Strength

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## Abstract

The Au stud bump, which is based on the wire bonding technology, offers a low cost flip chip solution for low I/O count ICs. The Au stud bumps were formed on the Al pads and coined to produce uniform bump height. Lead free 96.5wt%Sn3.5wt%Ag Solder paste was deposited on the Cu pads of the Printed Circuit Board (PCB) by stencil printing. The solder joints were fabricated by reflowing the solder paste after aligning Au stud bumps on the corresponding Cu pads. The solder joints were underfilled with epoxy. The strength of the joints before underfill was measured by die shear test.

Au-Sn intermetallic compounds were formed as a result of the Au stud reaction with Sn-Ag solder. Au-Sn intermetallic compounds spread over in the whole joints and the solder remained randomly as island shape due to the fast dissolution of Au into the solder.  $AlAu_4$  was formed as a result of the Au stud reaction with Al pad. The continuous layer of scallop-like Au-Cu-Sn intermetallic was formed at the solder/Cu pad interface. The microstructure of the solder joints did not change significantly even after multiple reflows and the thickness of the intermetallic layers increased with the number of reflows. The average shear force of the solder joints without underfill was very low. The fracture mainly followed the  $AlAu_4/SiO_2$  interface after the second reflow.

## Introduction

The trend toward higher speed and higher interconnect density for electronic packages is leading to the increasing use of flip chip technology. [1,2] In this high-density assembly technology, bare ICs are mounted facedown onto the substrate whereby the electrical interconnection is performed simultaneously via metal or conductive adhesive bumps. [3] Since established methods need expensive equipments and high operation cost, it is very important to reduce the cost.

Recently, the Stud Bump Bonding (SBB) method has been proposed as a very attractive solution for a low cost flip chip technology. [4-6] The process flow of the SBB process is shown in Fig. 1. The Au stud bumps are formed on each Al pads of a chip using the wire bonding technology. After Au stud bump formation, the Au stud bumps were flattened to make the bump height uniform. Solder paste is deposited on the substrate and then the chip is aligned on the substrate. After reflow process to make solder joints, the gap between the chip and the substrate is filled with underfill material. This technology has several advantages; Under Bump Metallurgy

(UBM) process is not necessary and fine pitch and chip level bumping is possible. [3,4]

The demand for low melting point solders at low cost and fine pitch organic substrates leads to eutectic PbSn solder being most commonly used. [7] However, due to environmental concerns, lead elimination from electronic products has been explored recently. [6-9] As an alternative to eutectic PbSn alloy, eutectic Sn-Ag solder is one of the candidate material.

The solder joints experience solder reflow cycles three or four times plus an additional underfill curing treatment. Repeated reflows affect the microstructure of the solder joints and the changes of the microstructure influence the reliability of the solder joints. So it is very important to study the microstructure of the solder joints as a function of the reflow cycles. [7]

In this study, the flip chip solder joints were fabricated using the Au stud bumps. The microstructural change in the solder joints was characterized using SEM, EDS, and X-ray mapping techniques and its effect on the mechanical reliability of the solder joints was also studied.

## Experimental Procedure

Test vehicles consisted of silicon test chip and printed circuit board. Substrate had peripheral Cu pads with solder mask and Si chip had the same number of Al pads of 7000 Å in thickness. The Au stud bumps were formed on each Al pads using a conventional wire bonding machine. Pb-free 96.5Sn3.5Ag solders were used to interconnect the Au stud bumps and the Cu pads on the substrate. SnAg paste was deposited on the Cu pads of the substrate by stencil printing. Prior to joining the chip and the substrate, the Au stud bump on the chip was aligned to the corresponding Cu pad in the substrate which had been printed with solder pastes. The interconnects were formed by reflowing the solder paste using an optimized temperature profile. Peak temperature was set at 30 degrees above the solder liquidus temperature and held for 69 seconds above the solder liquidus temperature. The reflow process was conducted 1, 2, 3, and 5 times to simulate the actual processing which included flip chip bonding and several rework process. The typical reflow profile is shown in Fig. 2.

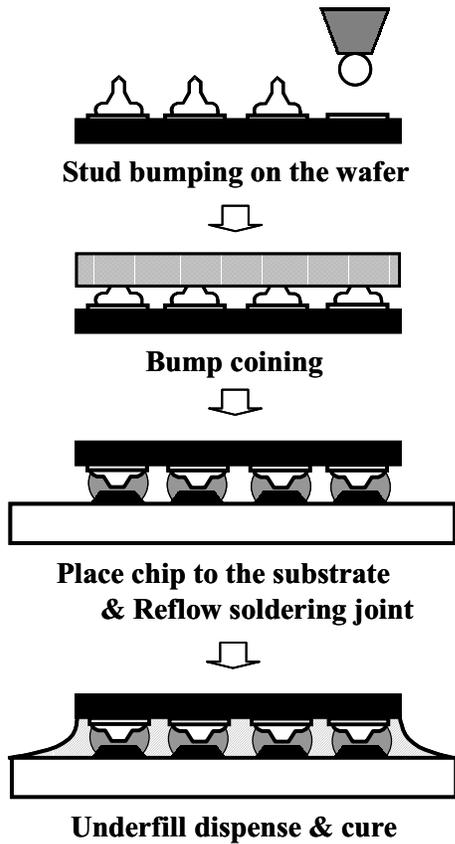


Fig. 1. Process flow of the SBB process.

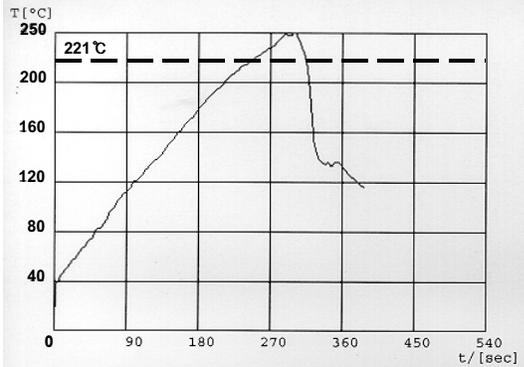


Fig. 2. Reflow profile of the SnAg test vehicles.

After flip chip solder joining, an underfill was applied to fill the gap between the chip and the board. To investigate the intermetallic formation and microstructure of the solder joints, the cross section of the solder joints were characterized using optical microscopy and scanning electron microscopy (SEM). The intermetallic compounds formed at the bonded interface were identified by energy dispersive X-ray spectroscopy (EDS). The intermetallic growth and microstructure of the solder joints were investigated as a function of the number of solder reflows.

Die shear test at the solder joints was also carried out by a commercial testing machine (HMP Soldermatics 1750 die shear tester) to measure the effects of the IMC on the reliability of solder joints. In this test, a tool pushed a chip

from one side, and a sufficient force was applied to push the chip off. The shear force was measured the maximum force needed to break the joints. The average shear force per each joint was calculated by the die shear force divided the number of solder joints in a chip. The shear force of the solder joints was measured as a function of the number of reflows. Underfill was not applied for this purpose. After die shear test, the fracture surfaces were examined by SEM. The intermetallic compounds of the fracture surfaces were identified by EDS.

## Results and Discussion

### *Microstructural observation of the solder joints*

Fig. 3 shows secondary electron images of the cross sections of solder joints with various reflow cycles. Au stud bumps on the chip and Cu pads on the substrate are connected by the solder. The gap between the chip and the substrate is filled with underfill. The morphology in each solder joint seems to be affected by the volume of the solder on each Cu pad. The macroscopic view of the solder joints was not changed due to multiple reflows. Even though the volume of the solder paste is not same in each joint, the solder joints were made successfully.

Backscattered electron images of the cross sections around the joints are shown in Fig. 4. After the first reflow (as jointed), Au diffused into the SnAg alloy and formed thick intermetallic layers and the solder remained randomly as an island shape due to the fast dissolution of Au into the SnAg solder. Multiple reflows did not change the elemental distribution according to these BE images. Fig. 5 shows the element distribution of the solder joints after the first reflow. According to this result, it was certain that Au diffused in the whole joints even in the first reflow cycle. It is well known that the diffusivity of Au into Sn is larger by several orders of magnitude than that of Sn into Au. [9] Thus, it is considered that solder was converted into Au-Sn intermetallic compounds by the reflow process.

The backscattered electron images of Au stud/solder interface are shown in Fig. 6. EDS analysis shows the  $\delta$ -AuSn,  $\epsilon$ -AuSn<sub>2</sub>, and  $\eta$ -AuSn<sub>4</sub> intermetallic compounds formation in the Au stud bump interface. The  $\delta$ -AuSn,  $\epsilon$ -AuSn<sub>2</sub>, and  $\eta$ -AuSn<sub>4</sub> intermetallic compounds having an irregular shape formed sequentially from the Au stud bump by interdiffusion of Au stud bump and SnAg solder. The  $\delta$ -AuSn and  $\epsilon$ -AuSn<sub>2</sub> phases thickened with reflow cycles. Fig. 7 shows the backscattered electron images of the Au stud/Al pad interface. Only one layer of intermetallic compound was formed after the reflow. EDS analysis shows that the intermetallic compound formed at the interface has a composition of approximately 83 at% Au and was identified as AlAu<sub>4</sub>. The AlAu<sub>4</sub> thickness was nearly constant even after multiple reflows. The Al pad was considered to be consumed completely after the first reflow. The backscattered electron images of solder/Cu interface are shown in Fig. 8. The formation of a ternary compound was observed. The continuous layer of scallop-like ternary Au-Cu-Sn intermetallic compound was formed at the solder/Cu pad interface. This ternary Au-Cu-Sn intermetallic compound is composed of 33 at% Cu, 22 at% Au, and 45 at% Sn,

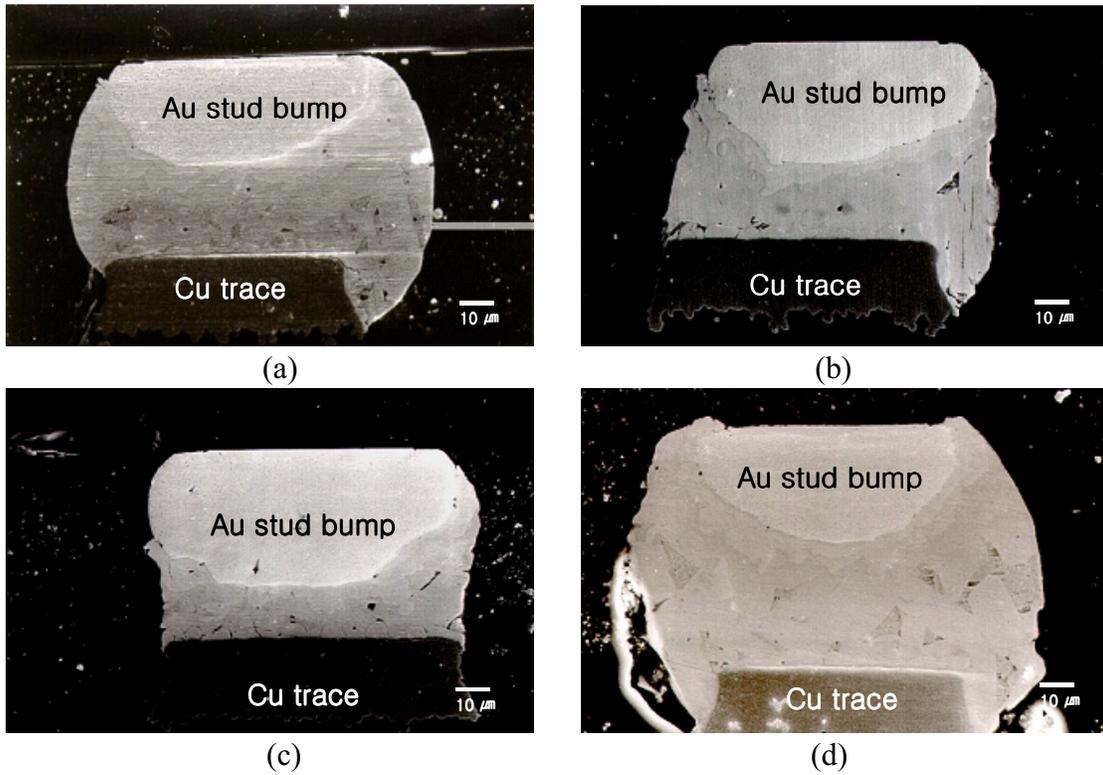


Fig. 3. Secondary electron images of cross section around the solder joints after (a) the first reflow, (b) the second reflow, (c) the third reflow, and (d) the fifth reflow.

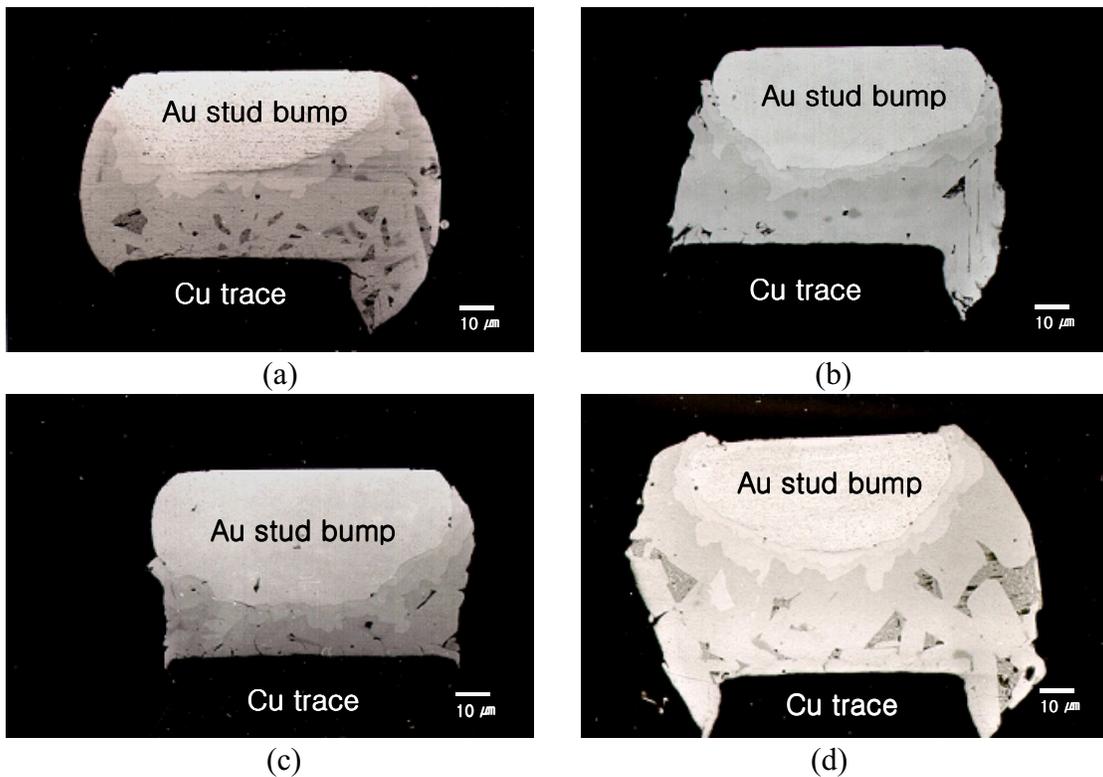


Fig. 4. Backscattered electron images of cross section around the solder joints after (a) the first reflow, (b) the second reflow, (c) the third reflow, and (d) the fifth reflow.

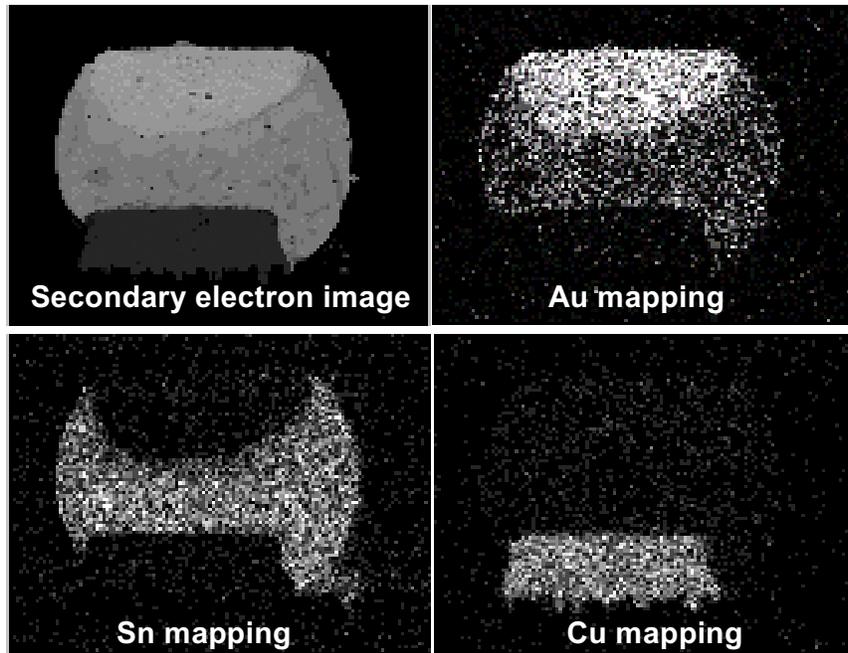


Fig. 5. X-ray mapping of the solder joints after the first reflow.

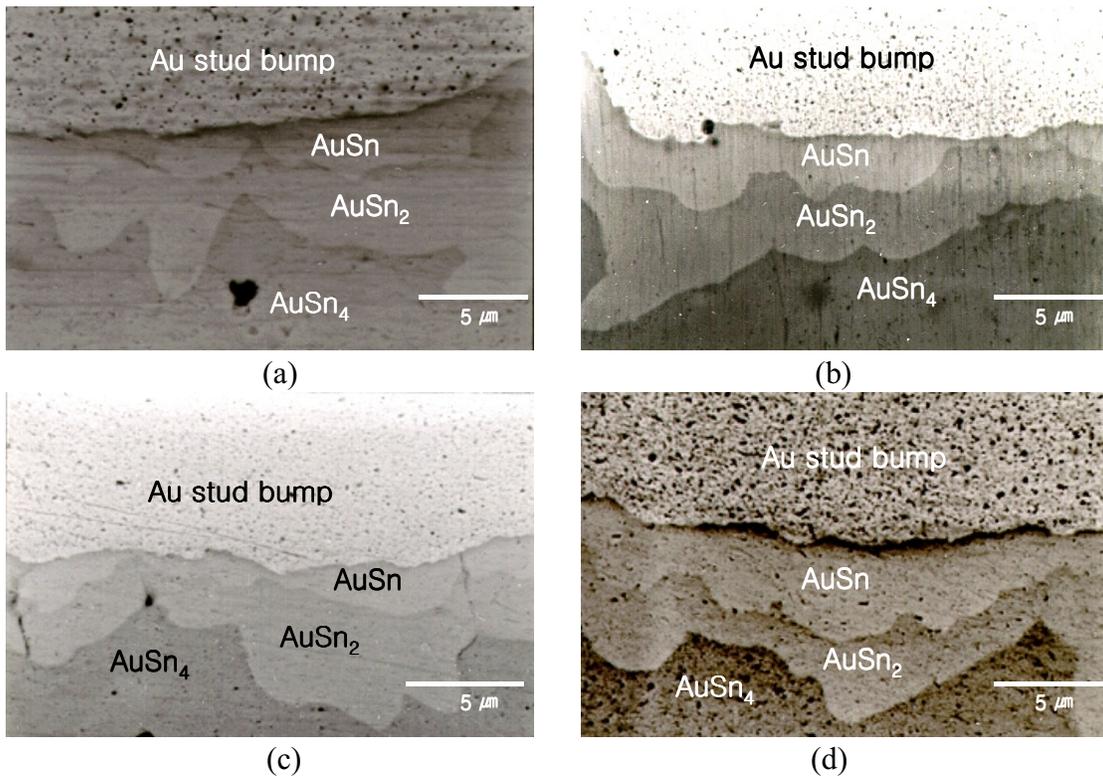


Fig. 6. Backscattered electron images of cross section around the Au stud/solder interface after (a) the first reflow, (b) the second reflow, (c) the third reflow, and (d) the fifth reflow.

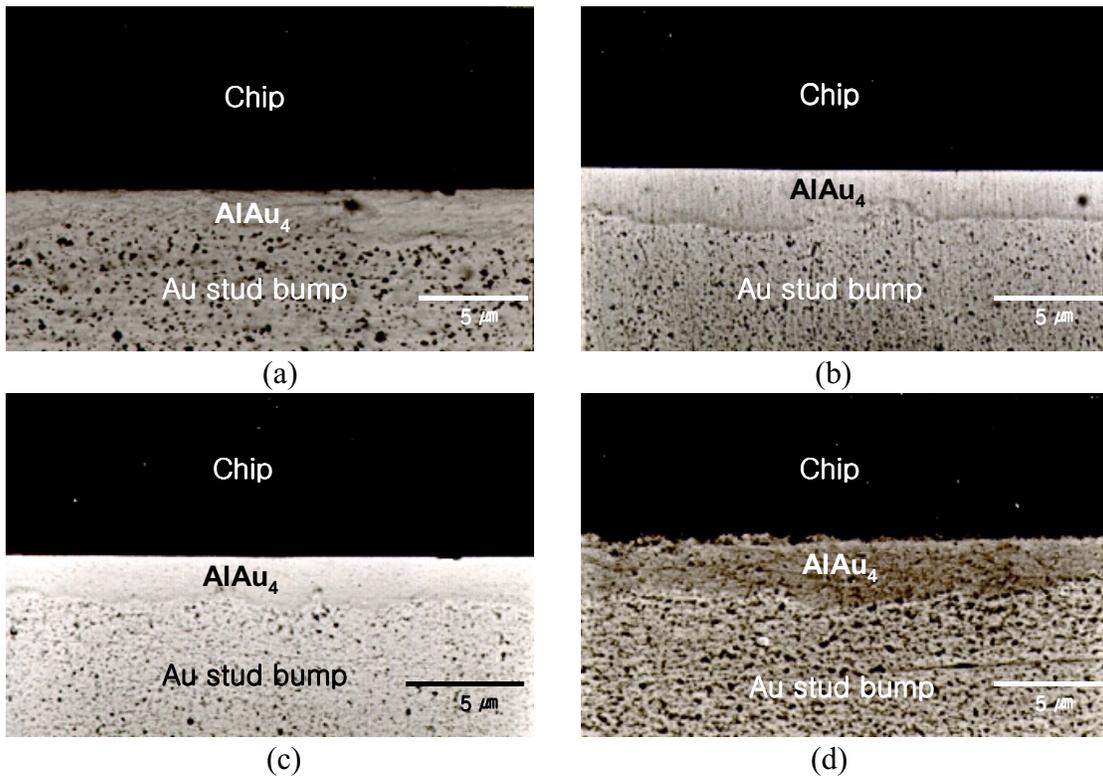


Fig. 7. Backscattered electron images of cross section around the Au stud/Al pad interface after (a) the first Reflow, (b) the second Reflow, (c) the third Reflow, and (d) the fifth reflow.

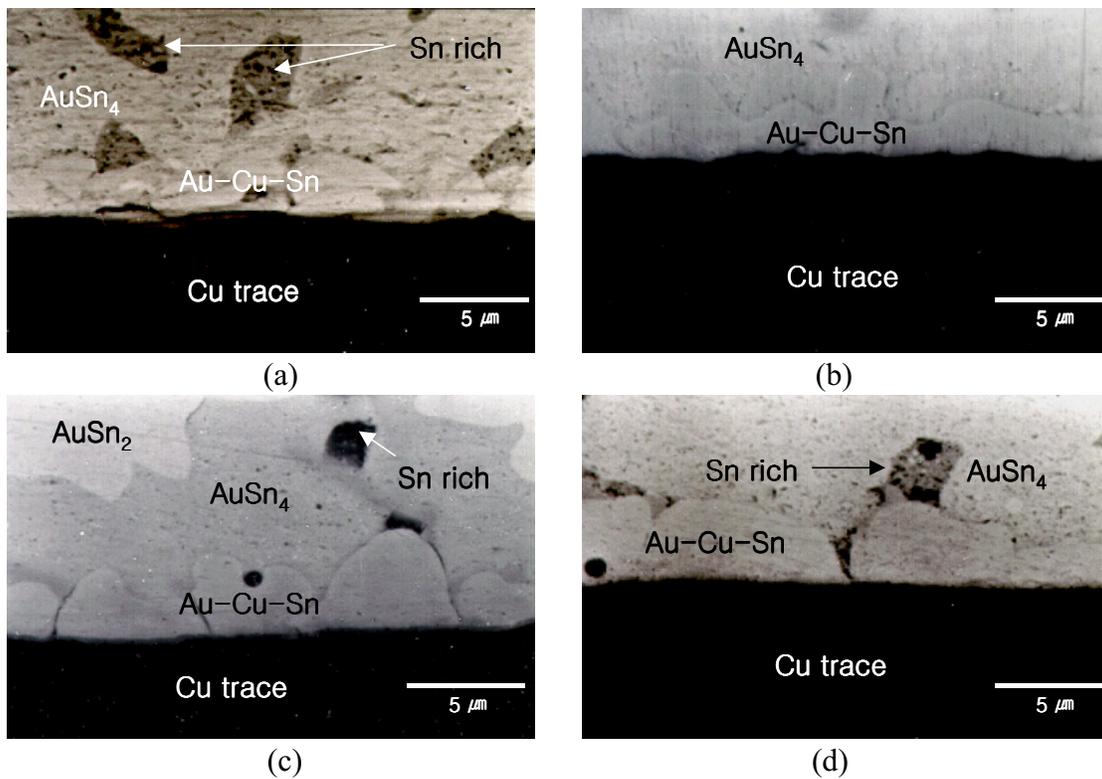


Fig. 8. Backscattered electron images of cross section around the Cu pad/solder interface after (a) the first Reflow, (b) the second Reflow, (c) the third Reflow, and (d) the fifth reflow.

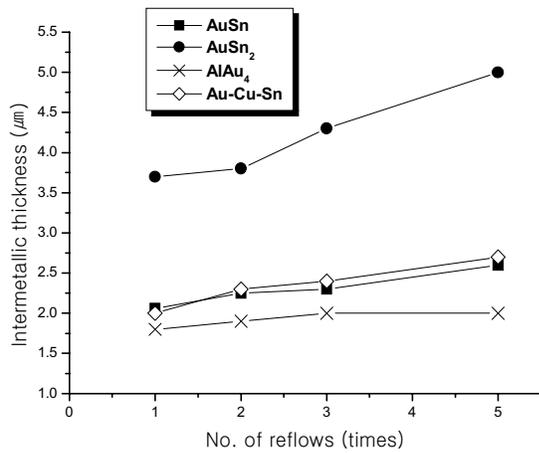


Fig. 9. The thickness of Intermetallic layers at various number of reflows.

approximately with (Au+Cu)/Sn ratio of 1.2. This indicate that this ternary compound is likely a  $\eta$ -Cu<sub>6</sub>Sn<sub>5</sub> type intermetallic.

The measured thickness of the AuSn, AuSn<sub>2</sub>, AlAu<sub>4</sub>, and Au-Cu-Sn is shown in Fig. 9. The thickness of the intermetallic layers increased with the number of reflows. The AuSn<sub>2</sub> phase grew faster than the other intermetallic layers. But the thickness of the AlAu<sub>4</sub> formed as a result of the Au stud reaction with Al pad nearly constant because most 7000 Å thick Al layer consumed during the first reflow process.

#### die shear test results

Fig. 10 shows the results of shear tests showing the average shear force as a function of the number of reflow cycles. The shear force remained almost constant with the number of reflows. No significant drop or increase was observed. The average shear force per joint without underfill was very low (about 8 gf).

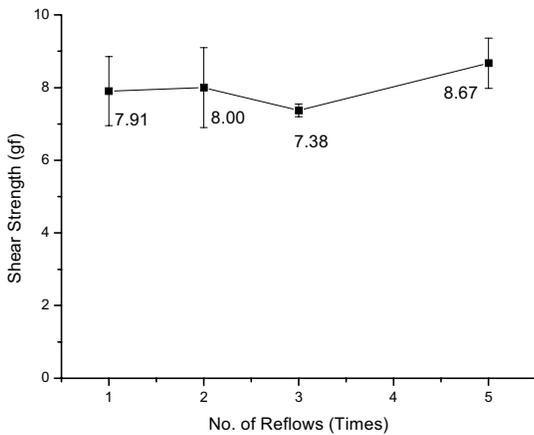


Fig. 10. The average shear force of the solder joints as a function of the number of reflows.

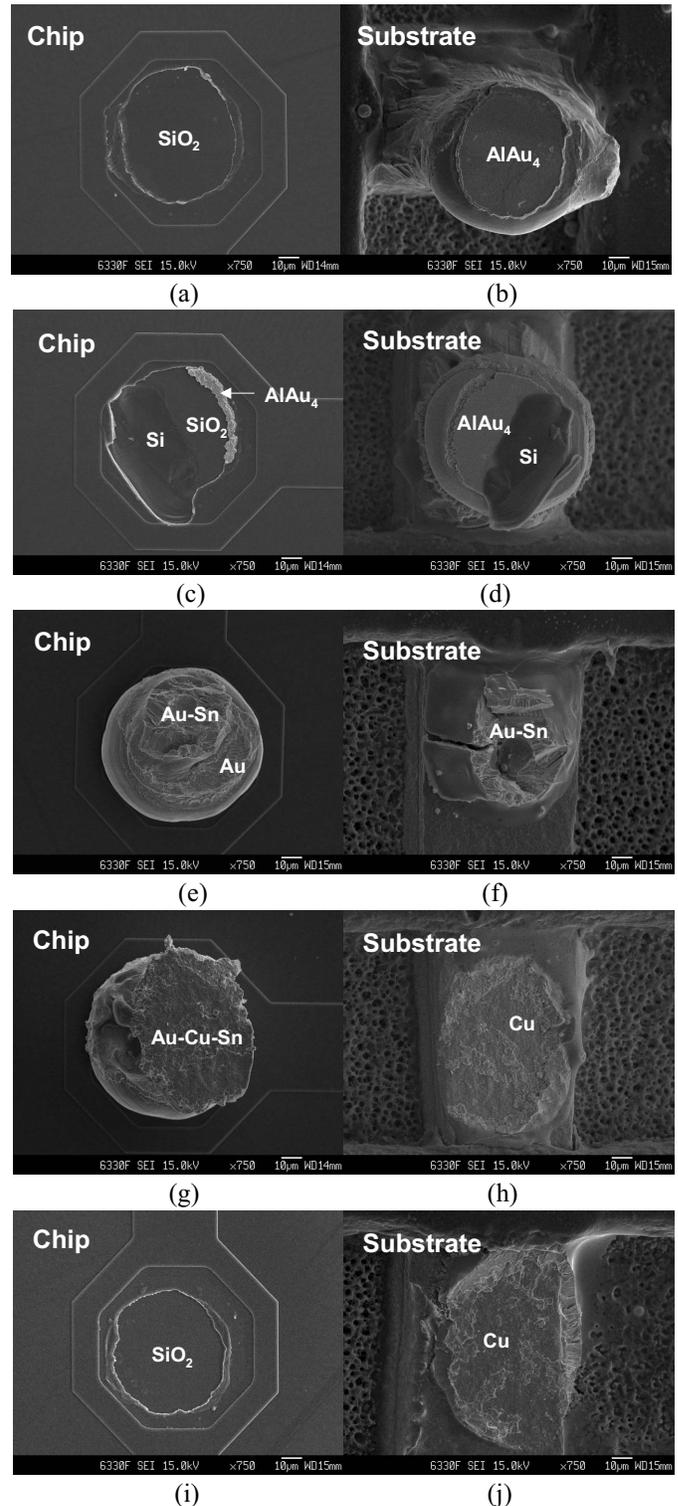


Fig. 11. Secondary electron images of the fracture modes after die shear test. (a)(b) mode A, (c)(d) mode B, (e)(f) mode C, (g)(h) mode D, and (i)(j) mode E.

Both the chip and the substrate side surfaces were observed in each fractured joint. The failure modes are summarized in Fig. 11 and 12. Mode A is the fracture occurred at the interface between AlAu<sub>4</sub> and SiO<sub>2</sub>. The SiO<sub>2</sub> surface is revealed on the chip, shown in Fig. 11 (a). AlAu<sub>4</sub> appeared on the substrate (Fig. 11 (b)). Fig. 11 (c) and (d)

show the fracture mode B. In mode B, the fracture occurred simultaneously inside the Si and SiO<sub>2</sub>/AlAu<sub>4</sub> interface. Fig. 11. (e) and (f) show the fracture mode C which occurred in the Au-Sn intermetallic compounds and the main fracture path was inside the AuSn<sub>4</sub> intermetallic compounds. It is well known that AuSn<sub>4</sub> intermetallic compound is very brittle. [6] Fig. 11 (g), (h) represent the fracture mode D which occurred in the ternary Au-Cu-Sn intermetallic compound on the Cu pad. Fig. 12 is the magnified image of the Fig. 11 (h). At the magnification, it was found that there are some residues of Au-Cu-Sn intermetallic compound on the top of Cu pad. Mode E is the fracture mode which occurred simultaneously at the SiO<sub>2</sub>/AlAu<sub>4</sub> interface and in the Au-Cu-Sn intermetallic. This mode is shown in Fig. 11 (i), (j).

Fig. 13 shows the percentage of each fracture mode. At the first reflow, the fracture mode C was commonly detected, but the main fracture mode did not exist. After the second reflow, mode A became the main fracture mode. Our results showed that most solder consumed and converted into intermetallic compounds in the whole joints after the first reflow. The intermetallic formation resulted in the brittle fracture. The shear force of the solder joint was very low. This weak strength of the solder joints due to the brittle intermetallic formation and the depletion of the soft solder layer in the whole solder joints can be a serious problem of the solder joints reliability.

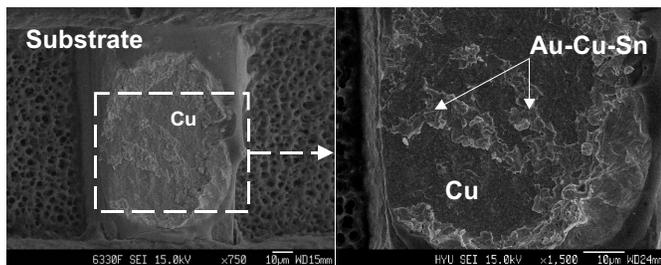


Fig. 12. Secondary electron image of substrate side - mode D.

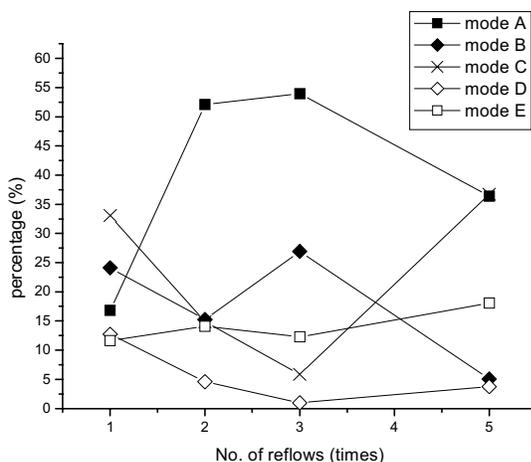


Fig. 13. The percentage of fracture mode as a function of the number of reflows.

## Conclusions

The flip chip solder joints were fabricated by using Au stud bump, SnAg solder paste, and Cu pads. The intermetallic formation in the solder joints was characterized and its effect on the shear force of the solder joints was studied. The main results are summarized as follows:

1. Au diffused in the whole joints to form Au-Sn intermetallics due to the fast dissolution of Au into the SnAg solder even after the first reflow.
2. AuSn, AuSn<sub>2</sub>, and AuSn<sub>4</sub> intermetallic compounds were observed as a result of Au stud reaction with Sn-Ag solder. The continuous layer of scallop-like Au-Cu-Sn intermetallic compound was formed at the solder/Cu pad interface.
3. Most Al layer in Al pad consumed after the first reflow process to form the AlAu<sub>4</sub> phase.
4. Even after multiple reflows, the microstructure of the solder joints did not change significantly.
5. The shear force of the solder joint was very low and almost constant with the number of reflows. This weak strength of the solder joints was attributed to the brittle intermetallic formation and the depletion of the soft solder layer in the solder joints.

## Acknowledgments

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# Assembly Process Issues in Integrating Commercial Reflow Encapsulants into Flip Chip Assembly

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## ABSTRACT

Reflow encapsulants introduce an alternative way to assemble flip chips other than the conventional use of flux spraying. Reflow encapsulants combine both the fluxing and underfilling, and are applied outside the placement machine, improving throughput and reducing manufacturing cost. During reflow soldering, some reflow encapsulants fully cure and therefore eliminate the post-curing process, thereby further reducing the manufacturing cost. Reflow encapsulants also eliminate the need for a nitrogen atmosphere during reflow.

There are many reflow encapsulants that are being sold commercially today. Although there are advantages associated with the use of reflow encapsulants, these materials introduce new issues to the assembly process. This paper discusses some of these issues in evaluating current commercial reflow encapsulants. Various reflow encapsulants from several vendors were used to build flip chip assemblies. The reflow encapsulants were evaluated for the effect of various process parameters, and their compatibility with the SMT assembly process. The process parameters included the placement force and hold time, and reflow profiles with various temperature settings and durations.

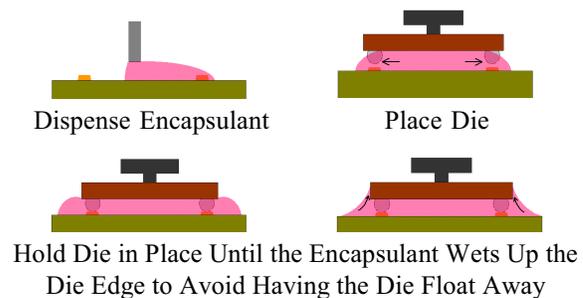
Many reflow encapsulants exhibited good soldering with the tested reflow profiles. Some of the reflow encapsulants gelled during high temperature soak, preventing solder bumps from properly soldering onto the substrate pads. No die floating or shifting was observed with various placement settings. A reflow encapsulant containing filler particles had soldering defects that were caused by the presence of these filler particles.

## INTRODUCTION

Reflow encapsulants introduce an alternative way to assemble flip chips other than the conventional use of flux spraying. With the spraying method, the die sites are sprayed with liquid flux prior to chip placement. Following the reflow soldering of the joints, the flip chips are then underfilled by capillary flow using a dispenser. Fluxing within the placement machine and dispensing of the underfill not only reduce throughput, but also increase the manufacturing cost of the flip chip assembly [1]. Reflow encapsulants, on the other hand, combine these two steps and are applied outside the placement machine, improving throughput and reducing manufacturing cost. They provide the fluxing activity required for solder bumps to form joints, act as the underfill to distribute the thermal stress induced by the CTE mismatch [2], and eliminate the concerns for compatibility of individual fluxes and underfills. The reflow encapsulants are dispensed on the substrates outside the placement machine at room temperature. During reflow soldering, some reflow

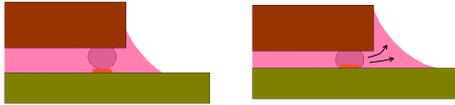
encapsulants fully cure and therefore eliminate the post-curing process, thereby further reducing the manufacturing cost. Reflow encapsulants also eliminate the need for a nitrogen atmosphere during reflow.

There are many reflow encapsulants that are being sold as mature products today. Although there are advantages associated with the use of reflow encapsulants, these materials introduce new issues to the assembly process. With the use of reflow encapsulants, the substrates must be dry prior to assembly. The presence of moisture results in underfill voids under the die and may also change the material's cured properties. The dispensing pattern should be carefully considered to prevent the entrapment of voids during placement and to have a better control of the fillet thickness. During placement, the reflow encapsulant needs to flow out from under the chip and wet up the sides of the chip as shown in Figure 1. The placement force provides pressure to place the die on the dispensed material. In addition, a hold time is



**Figure 1. Reflow Encapsulant Dispense and Placement**

used to hold the die for a specified time, to allow the material to wet up the die edge before being released. The placement force and hold time should be optimized to ensure that the chip does not float on the dispensed material or shift away from the pads. Both soldering and curing of the reflow encapsulant occur during reflow. As the solder bumps collapse during reflow, the encapsulant should remain fluid to allow the die to be pulled down to the substrate pads by the liquid solder joints as shown in Figure 2. The material must not gel before reflow, as this prevents the solder bumps from forming joints on the substrate pads [3]. After the formation of the solder joints, the reflow encapsulant fully or partially cures before it exits the reflow oven. Some reflow encapsulants can be used with “standard” SMT reflow profiles, but some require reflow profiles without a soak to prevent premature gelling. It is preferable to have a reflow encapsulant that can use a “standard” reflow profile in order to integrate the flip chip with SMT.



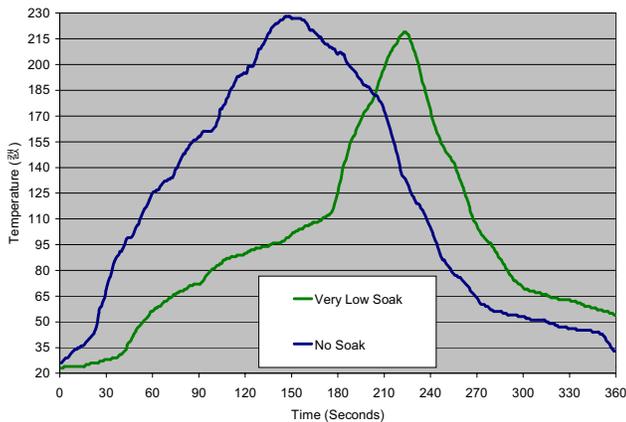
Material Must Remain Fluid Until the Solder Reflows and Joins with the Pad, and then the Material Must Flow Out from Under the Die During Collapse

**Figure 2. Second Flow of Reflow Encapsulant During Reflow**

## EXPERIMENTAL DESIGN

### Reflow Encapsulants

Ten commercially available reflow encapsulants from several vendors were used to build flip chip assemblies. Five of the ten reflow encapsulants did not require a post-cure cycle whereas five did. While most reflow encapsulants are unfilled, one encapsulant contained silica filler particles. Filler particles are added to lower the CTE of the material [4]. Furthermore, two reflow encapsulants had supplier recommended reflow profiles that had either no soak or very low soak (Figure 3). One reflow encapsulant had a very high reported viscosity of 1,900,000 cP (1,900 Pas).



**Figure 3. Supplier Recommended Reflow Profiles of Very Low Soak and No Soak**

### Test Vehicle

Flip chips were assembled to a 62 mil thick test board made with high  $T_g$  (170°C) FR-4. The substrate had a popular solder mask and electroless Ni/Au pad finish. The chip used measures 200 x 200 mils (5.08 x 5.08 mm) and is 25 mils (0.64 mm) thick. The 88 eutectic Sn/Pb solder bumps are arranged in a single perimeter row with an 8 mil (0.20 mm) pitch. The chip passivation is silicon nitride. The pads are formed by 3 mil (0.08 mm) wide traces running through a 7 mil (0.18 mm) wide trench solder mask opening.

### Assembly Process

The assembly process included baking out the substrates, dispensing reflow encapsulant, die placement, reflow soldering and curing, and post-curing when recommended.

The study of these reflow encapsulants concerns two aspects of assembly. The first involves the two placement parameters, placement force and hold time. In the Universal Instruments' GSM placement machines, hold time is varied with the "delay before air kiss" parameter. This is the delay between the application of the load and the release of the nozzle vacuum. The second part of the experiment studied the effect of various reflow profiles on soldering.

### Substrate Bakeout

Die were assembled on a substrate that was baked out either at 125°C for two hours or baked through one reflow pass. The reflow pass had a peak temperature of 224°C, soak temperature of 157°C, and 195 seconds to 183°C. Assembly occurred within five minutes of the bakeout in order to cool the substrate down to room temperature.

### Reflow Encapsulant Dispensing

Reflow encapsulants were dispensed using an automatic commercial underfill dispenser. The reflow encapsulant was thawed at room temperature for at least an hour prior to dispensing. The reflow encapsulant was dispensed as a dot of 6.5mg at the center of the die site with the needle 10 mils (0.25 mm) above the board. A 25 gauge needle with a polypropylene hub and a stainless steel tip was used. The needle had an inner diameter of 10 mils (0.25 mm) and outer diameter of 20 mils (0.51 mm). No substrate or material heating was required.

### Die Placement

The flip chips were placed using a Universal Instruments GSM linear motor placement machine. The default placement settings are 150g of placement force and 30ms of hold time. Initially, 750g of placement force and 300ms of hold time were used. Then the hold time and placement force were decreased to either the default settings, or the default hold time and 300g of placement force. For the investigation of the reflow profile sensitivity, placement settings of 300g of force and 300ms of hold time were used.

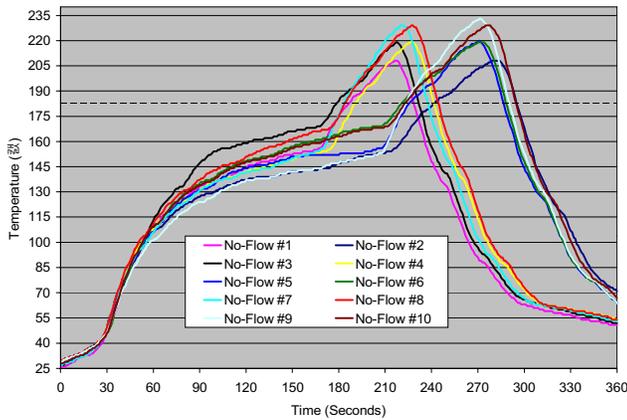
### Reflow Soldering/Curing

A Vitronics Soltec XPM730 forced convection oven with seven heating zones was used to reflow solder and cure these assemblies. Ten reflow profiles were used to evaluate the soldering process window for all of the ten reflow encapsulants. These profiles had soak temperatures ranging from 154°C to 172°C, peak temperatures from 208°C to 233°C, and times to 183°C from 183 to 241 seconds. The reflow profiles are shown in Figure 4. These profiles map out a "standard" SMT reflow process. Each reflow profile was developed and verified using a MOLE ThinLine reflow profiler. Two die were assembled for each reflow profile. Assemblies were reflow soldered in air without the use of nitrogen.

## RESULTS AND DISCUSSION

### Placement Force and Hold Time

For five reflow encapsulants, the die placed with the default placement force of 150g and the default hold time of 30ms were electrically continuous, and no shifting or floating



**Figure 4. Reflow Profiles Used in the Reflow Profile Sensitivity Study**

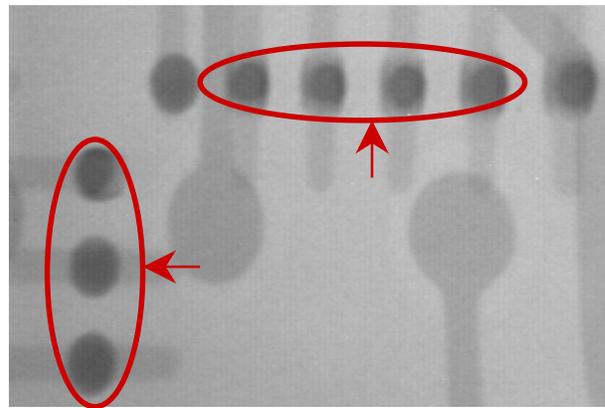
of the die was observed. Similarly, for four other reflow encapsulants, the die placed with 300g of placement force and the default hold time of 30ms were also electrically continuous with no placement related defects were observed. Both sets of the placement settings used here, the default settings and the 300g of force and 30 ms of hold time, give a faster throughput than the typical settings used for dip fluxing. However, one reflow encapsulant, having a very high viscosity, required a higher placement force and hold time of 500g and 500ms, respectively. Using lower settings resulted in chips floating off the substrate pads.

**Reflow Profile Sensitivity**  
**Soldering**

Seven of the ten reflow encapsulants gave good soldering with the tested reflow profiles, indicating a wide reflow process window. The remaining three reflow encapsulants also gave good soldering but had a narrower reflow process window, indicated by the sensitivity to soak temperature and time.

One of these three reflow encapsulants was sensitive to soak temperature and time while peak temperature in reflow did not affect it. This encapsulant was especially sensitive to reflow profiles that had high soak temperature and longer soak time, resulting in electrical opens and high resistances. While the material provided good soldering, the high soak temperature and longer duration caused the underfill to gel before all solder joints could form. For this particular reflow encapsulant, a cooler reflow profile would be the conservative choice, but this could be an issue for integrating the flip chip and SMT since a flip chip reflowed with SMT components would normally experience a hotter reflow profile.

An X-ray imaging system was used to observe the solder defects in this material. For reflow profiles with high soak temperature, many of the solder joints have not soldered at all as shown in Figure 5. These sit on top of the pad and appear round and dark gray. The few solder bumps that did wet the substrate pads do not appear round. In a cross-section of one of these assemblies, we did find that all solder bumps sit on top of the substrate pad regardless of whether any solder wet to the pad or not, as shown in Figure 6. Essentially, the gelled material prevented a complete collapse of these solder joints for these reflow profiles. For comparison, the lower soak



**Figure 5. X-Ray Image of Limited Soldering with High Soak Temperature Reflow Profile Assembly**

profiles gave complete collapse onto the substrate pads as shown in Figure 7.



**Figure 6. Partially Soldered Joints in a Die Assembled with High Soak Temperature Reflow Profile**



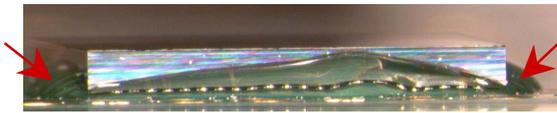
**Figure 7. Good Soldered Joints in a Die Assembled with Low Soak Temperature Reflow Profile**

As mentioned previously, two reflow encapsulants had reflow profiles that were recommended by the manufacturers. One of the two reflow profiles was characterized by a very low soak, and the other was a "volcano" profile with no soak. Assemblies built using the reflow encapsulant with the recommended low soak reflow profile fluxed and soldered. Although two "standard" SMT profiles with low temperature soaks also fluxed and soldered well, underfill voids caused assembly defects and the assembly evaluation ended without testing hotter profiles.

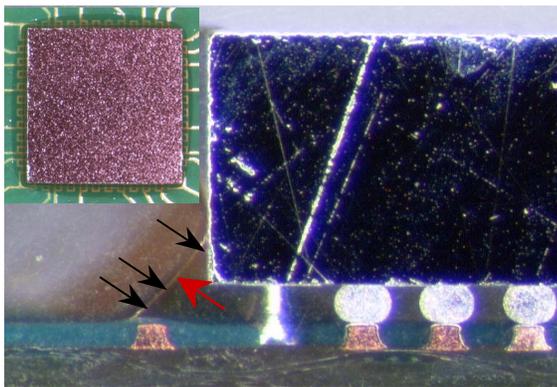
The reflow encapsulant with a "volcano" reflow profile also resulted in a narrower reflow process window. The assemblies had soldering defects that were associated with the sensitivity to a soak. Using a "standard" SMT reflow profile that had a low temperature and long soak, the assemblies had high electrical resistance and opens. A longer soak had gelled the underfill before solder joints could have formed. However, good soldering results were achieved with the SMT reflow profiles of low temperature and short soak.

### ***Fillet Formation and Premature Gelling of the Underfill***

Evidence of premature gelling causing solder defects was also observed in the fillets around the chip with one reflow encapsulant. As discussed earlier, the reflow encapsulant must be fluid when the solder joints form. As the solder bumps collapse onto the substrate pads, the chip is pulled towards the substrate and encapsulant is squeezed out into the edge fillets. If the fillet surface gels, the encapsulant will not be fluid enough to form smooth fillets. Instead, the fillets around the chip will stretch and bulge to accommodate the material squeezed from under the chip. This was observed for a reflow profile with a high temperature and longer period soak as shown in Figure 8. Another sign of gelling is the assemblies having thin, smooth fillets as shown in Figure 9. This is also due to high temperature and longer soak, causing premature gelling to prevent collapse with no material squeezed from under the chip.



**Figure 8. Bulging Fillets Around the Edges of a Die Assembled with High Soak Temperature Reflow Profile**



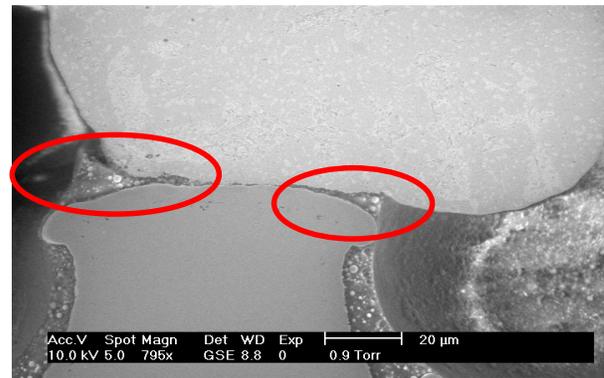
**Figure 9. Thinner Fillets Around a Die Assembled with High Soak Temperature Reflow Profile Due to Limited Solder Joint Collapse**

### ***Filler Particles***

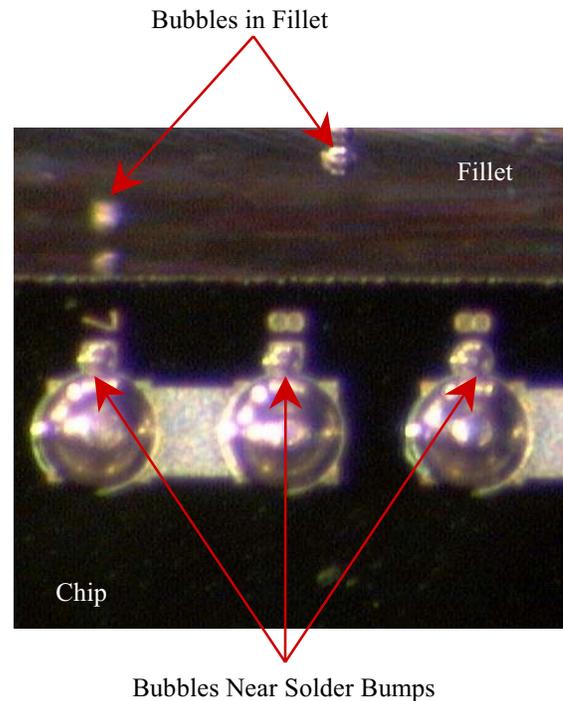
A reflow encapsulant containing filler particles to lower the CTE soldered well, however, many of the assemblies built using this reflow encapsulant had solder bridges and limited soldering. Unlike the premature gelling of the other underfills, the filler particles contained in the reflow encapsulant were the cause of the soldering defects. In Figure 10, the cross-section image of a partially soldered bump has been enlarged to show the filler particles between the solder bump and the substrate pad. These filler particles had prevented the solder bumps from collapsing onto the substrate pads.

### ***Fillet Bubbles***

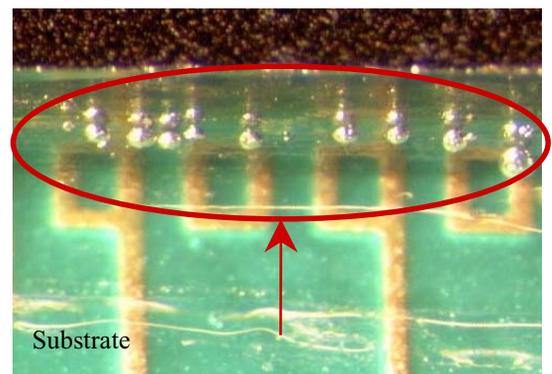
Many bubbles were observed in the fillets around the die with few reflow encapsulants. Die were placed on glass slides,



**Figure 10. Limited Soldering Caused by the Filler Particles Between the Solder Bump and the Substrate Pad**



**Figure 11. Placement Bubbles Next to Solder Bumps in a Chip Placed on a Glass Slide**



**Figure 12. Bubbles in Fillets After Reflow Soldering**

then the slides were inverted to observe the material. A small bubble was observed on the “leeward” side of each solder bump, the side closest to the edge of the chip. This is caused by the flow of the reflow encapsulant around the solder bumps during chip placement. These bubbles were smaller than the solder bumps, roughly 1 mil (25.4  $\mu\text{m}$ ) in diameter. Figure 11 shows placement bubbles next to solder bumps in a chip placed on glass slide. If these bubbles do not dissolve during reflow, the bubble is often pushed out from under the chip and into the fillet when the solder joints collapse as shown in Figure 12.

#### Underfill Voids

Many underfill voids were observed with several reflow encapsulants. The C-mode Scanning Acoustic Microscope (C-SAM) images of underfill voids for some of the reflow encapsulants are shown in Figure 13. Since the substrates were baked prior to assembly, the underfill voids should not be moisture related, but may be caused in die placement or by the outgassing of the material during reflow.

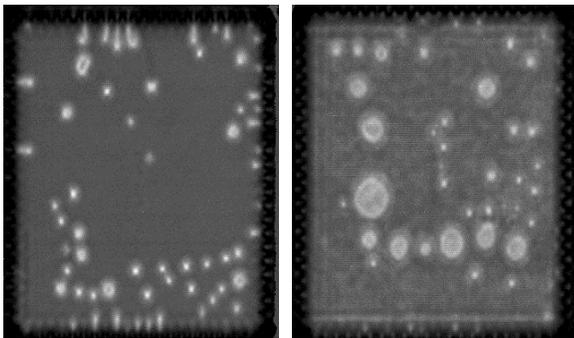


Figure 13. C-SAM Images of the Underfill Voids

#### Mechanical Stability of "Cured" Underfill

Evidence of unstable curing of one reflow encapsulant was observed when more assemblies were built on the same substrate and were passed through subsequent reflows and post-cure cycles. Immediately after the post-cure cycle, it was observed that a bubble observed previously near the edge of the chip had moved and another bubble had appeared during the subsequent reflow and post-cure cycle, as shown in Figure 14. The movement and the growth of the fillet bubbles indicate that the reflow encapsulant material was not stable even after multiple passes through a reflow oven and the post-cure cycles. The mechanical instability of this reflow encapsulant is a reliability concern since the encapsulant will not provide adequate protection to the solder joints.

#### CONCLUSION

Ten reflow encapsulants were used to build flip chip assemblies with various process conditions for die placement and reflow profiles. The placement hold time and load were acceptable for flip chip assembly with throughput competitive with the flux dipping method. The reflow profile sensitivity study indicated that many of the commercial reflow encapsulants can be reflow soldered using "standard" SMT reflow profiles, but some may be sensitive to higher soak temperatures, resulting in either unformed or cold joints. The

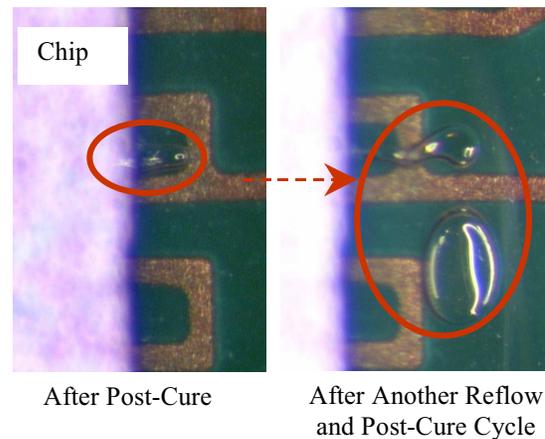


Figure 14. Movement and Growth of Fillet Bubbles In Subsequent Reflows and Post-Cure Cycles

sensitivity to reflow temperatures may lead to difficulty in integrating the flip chip assembly with SMT. Filler particles contained in a reflow encapsulant also caused soldering defects, which prevented solder bumps from collapsing onto substrate pads.

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# Interfacial Reaction of Printed Solder Bump with UBM

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## Abstract

This work is to investigate the interfacial interaction between the UBM and solder bump produced with print bumping process. The solder bump manufactured with printing by using PI (polyimide) as the patterning mask was investigated for its interfacial reaction with electroless nickel UBM. The solder paste is a 63Sn-37Sn solder with 90% of metal content. The solder powder is of type 5 with particle sizes range from 15  $\mu\text{m}$  to 28  $\mu\text{m}$ . Reflow of the solder paste was conducted at 230 °C for 30 sec. The electroless nickel was deposited on Cu electrode of silicon chip. A thin layer of electroless Au was deposited on the electroless nickel to provide wetting property and oxidation resistance for the electroless nickel. The solder bump was tested, respectively, under 150 °C and 85 °C /85RH for up to 1000 hours. The interdiffusion behavior of the constituent elements Cu, Ni, and Sn across the interface was investigated with elemental line scanning. It was found that the electroless nickel with a thickness of 5  $\mu\text{m}$  functions well as a diffusion barrier for Cu and Sn. No interdiffusion was seen between Cu and Sn after 1000 hours of test under the two testing conditions. At least 60% of the original thickness of electroless nickel was found left after testing. The intermetallic compounds formed at the interface were investigated by etching off the unreacted solder. The compounds grow with increasing testing period as would be expected. The compound was also characterized with XRD and SEM to reveal the compound phase and microstructure. There is only one intermetallic compound,  $\text{Ni}_3\text{Sn}_4$ , detected at the interface under the testing condition.

## 1. Introduction

Flip chip solder bump can be produced by means of evaporation, electroplating, or printing. Evaporation method uses a metal mask to define the pattern, while the electroplating method applies photoresist (1) to define the pad area for solder deposition. The bump height uniformity of electroplated solder bump is governed by bump position on a wafer (1) as the current distribution is a position function. A suitable design of electroplating cell can significantly even out the current distribution and thus eliminate the position effect on bump height uniformity (2). The growth rate of electroplated solder bump is also governed by several factors such like current density and bath type (3). In contrast to the complicate controlling factor of electroplating bumping process, the currently commercialized printing process conducts lamination of dry film followed by lithography to

allocate the bump opening wherein solder paste is filled by conventional printing step.

The printing process provides high throughput and easy control of bump height. It is a primary choice of some industry people. Yet, it suffers from the relatively large pitch area and pad size. At current stage, the difficulty to reduce bump and pitch sizes is partly due to the large powder size of solder paste, sticky of paste, and mask fabrication. The metallic stencil still encounters limit to opening dimension. This difficulty restricts the bump pitch and bump dimension. Patternizable polyimide has been discussed for electronic packaging application (4). Polyimide, due to its photosensitive characteristic, could simplify the bumping process and provide the passivation for redistributed circuits. Humidity absorption and inadequate practical experience are part of the reason why polyimide has not been widely applied in packaging industry. It has been developed in the laboratory a bumping process applying patternizable polyimide for printing mask. The purpose of this work is to investigate the interfacial interaction of the printed solder bump with electroless nickel under bump metallurgy.

## 2. Experimental Procedure

The print bumping process starts from P-type 4" silicon wafer. UBM for solder bump was produced with lithography method. The pad is 100  $\mu\text{m}$  diameter circular in dimension. The pitch size is 250  $\mu\text{m}$ . The pattern consists of 21 x 21 chips with 19 x 19 bumps on each chip. The silicon wafer was sputtering deposited with Ta/TaCu/Cu multilayer with a thickness of roughly 3000~4000 Å each. Electroless nickel, 5  $\mu\text{m}$ , was then deposited on the Cu layer, followed by electroless Au of 1000 Å. The Cu pad was activated with DMAB (dimethylamine borane) prior to electroless nickel deposition. The electroless nickel deposition was conducted at pH 4.6 with a temperature of 83 °C in a nickel sulfate solution (5). The electroless Au was deposited, conducted at pH 7.0 and 90 °C, in a solution containing 2 g/l gold potassium cyanide, 75 g/l ammonium chloride, 50 g/l trisodium citrate dihydrate, and 10 g/l sodium hypophosphite.

Figure 1 represents the structure of the solder bump produced with printing. The PI (polyimide) layer, Lithography (I) in Figure 1, is a positive PI of which the thickness is 2 $\mu\text{m}$  before curing. The second layer of negative PI, Lithography (II) of Figure 1, was spin coated on the cured positive PI to give a desired thickness. The opening has a diameter of 150  $\mu\text{m}$ . A commercial solder paste of 63Sn-37Pb was then printed to fill the openings. The powder size of the

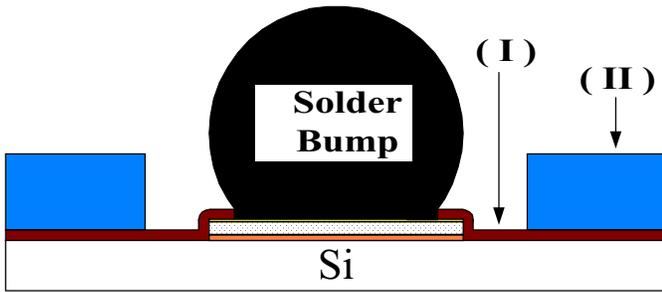


Figure 1 Structure of print solder bump with passivation

as supplied solder paste is Type 5, 20~25  $\mu\text{m}$ . Reflow of the solder paste was conducted in an IR (infrared) furnace with programmable heating profile. The optimum reflow temperature is 230  $^{\circ}\text{C}$ .

The solder bump was aged under 150  $^{\circ}\text{C}$  or at 85  $^{\circ}\text{C}$  /85%RH (relative humidity) for up to 1000 hours. The cross section of the solder bump was investigated with SEM (scanning electron micrograph) for the intermetallic compound formed at the interface. The unreacted solder bump was etched off to reveal the intermetallic compound. The intermetallic compound was further characterized with XRD (x-ray diffractometry).

### 3. Results

Solder paste consists of solder powder and organic flux. Flux will vaporize during reflow and the solder powder melts to bond with the UBM of solder bump. It is known that the vaporization of flux may result in formation of void after solidification. Figure 2 represents the microstructure of a

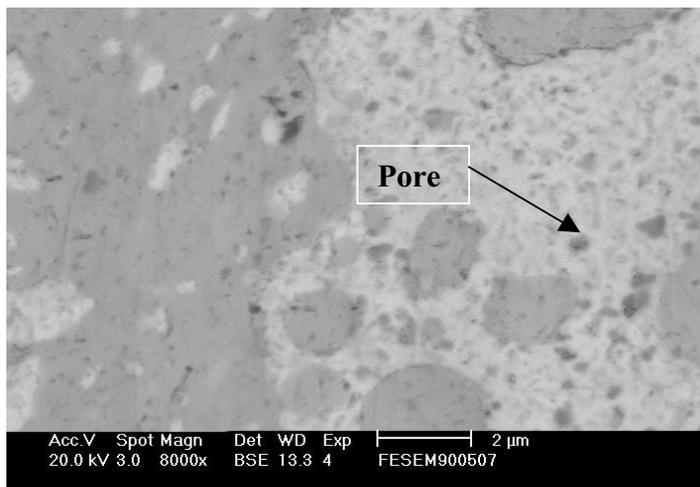


Figure 2 Metallurgraph of reflowed solder bump showing existence of sub-micron pores.

solder bump produced in this work. Voids of sub-micron size are evidently observed especially associated with the Pb-rich phase, the white phase in the picture. In view of this observation, it is of interest to investigate if the void exists at the interface and how does it affect the interaction between solder and UBM.

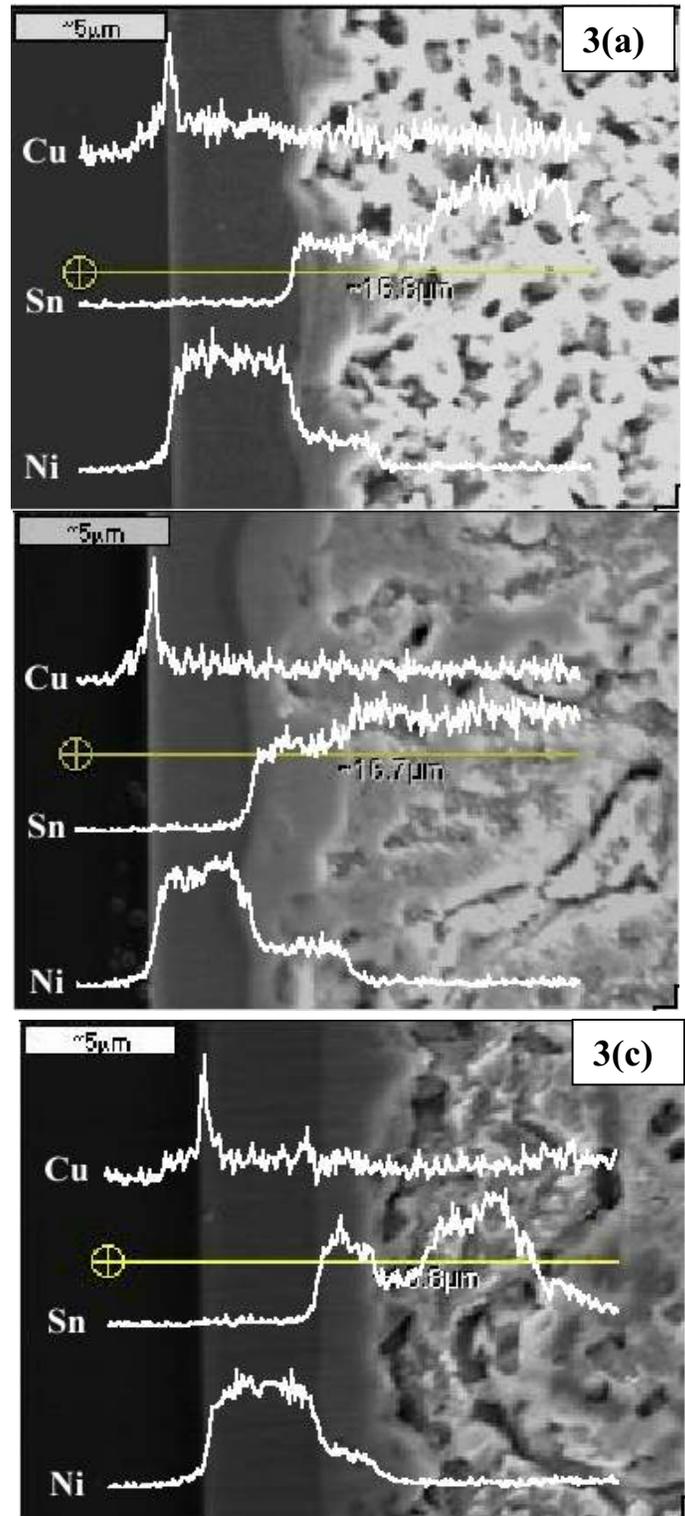


Figure 3 Elemental analysis across the interface of solder bump (a) as reflowed, (b) after aging at 150  $^{\circ}\text{C}$  for 1000 hours, (c) after humidity test at 85  $^{\circ}\text{C}$  /85RH for 1000 hours.

The Au layer is rather thin of which the purpose is to protect the UBM from oxidation as well as to provide the needed

wettability. It is known that Au reacts rapidly and exhibits good solubility with Sn. Accordingly, the Au layer is not observable after reflow. It is even not detectable after reflow as having been diluted. The main elements being able to be detected will not include Au. Meanwhile, Pb is not known of having any reaction with the UBM materials of this study. The interfacial analysis thus focuses on Cu, Sn, and Ni elements. Figure 3(a) presents the cross sectional analysis of as reflowed solder bump. Cu stays close to Si underneath the Ni layer. A nickel layer with a thickness of around  $5\mu\text{m}$  is observed. It is also observable that there exists a layer between the Ni layer and the solder. This intermediate layer is mainly composed of Ni and Sn. The thickness of this layer is around  $2\mu\text{m}$ . In regarding to the concern of the effect of flux vaporization on the interfacial interaction, it is evident that no void is observed at the interfacial region. Apparently, the vaporization of flux during reflow does not show particular impact on the interfacial interaction.

The electroless nickel deposit applied in this work as diffusion barrier contains 5.6%P and has a thickness of  $5\mu\text{m}$ . The deposit is a crystalline structure. There has been a concern on applying the crystalline structure as diffusion barrier for it contains grain boundary. However, all analysis, Figures 3(a)~(c), show that the  $5\mu\text{m}$  deposit can withstand reflow as well as both long time testing conditions of this study. Copper and Sn still stay at least  $4\mu\text{m}$  away from each other. With the solder paste, it is observable from Figure 3(a) that a compound layer is formed between Sn and Ni right after reflow, evidenced by the plateaus on both elemental lines of Ni and Sn. The thickness of this compound layer ranges from 2 to  $3\mu\text{m}$  for the as reflowed solder bump.

Aging at  $150^\circ\text{C}$  and  $85^\circ\text{C}/85\text{RH}$  do enhance the growth of the intermetallic layer. The intermetallic compound formed after aging for 1000 hours can be as thick as  $4\mu\text{m}$  for both testing conditions. In the meantime, there has at least  $3.5\mu\text{m}$  of electroless nickel deposit left. In other words, the electroless nickel consumed at most  $1.5\mu\text{m}$  to produce the  $4\mu\text{m}$  intermetallic compound. This result indicates that Sn diffuses faster than Ni during compound formation. This is anticipatable as the melting point of electroless nickel,  $895^\circ\text{C}$ , is higher than that,  $183^\circ\text{C}$ , of solder.

1000 hour of high temperature aging or humidity test results in growth of only around  $2\mu\text{m}$  in thickness, in comparison with as reflowed solder bump, of compound layer. However, the grains of the compound tremendously grow after the aging. The grain size of the compounds formed after reflow can range from 0.5 to  $8\mu\text{m}$ , Figure 4(a). Yet, a great population of the grains is of fine size. On the other hand, the fine grains grow after 1000 hours of both testing, Figures 4(b) and 4(c). The fine columnar grains observed in Figure 4(a) are no more observed in Figures 4(b) and 4(c). It is also of interest to notice that the compound crystals are loosely distributed within the compound layer of the as reflowed solder bump, Figure 4(a). However, these crystals are densely and compactly stacked after 1000 hours of testing, Figures 4(b) and 4(c), especially for aging at  $150^\circ\text{C}$ . This observation indicates that a tremendous number of compound nuclei are formed during reflow. These nuclei then grow during the

reflow or the long time testing period. The growth of the compounds tends to round off the sharp edge of the crystals so as to lower the surface energy. The compound growth

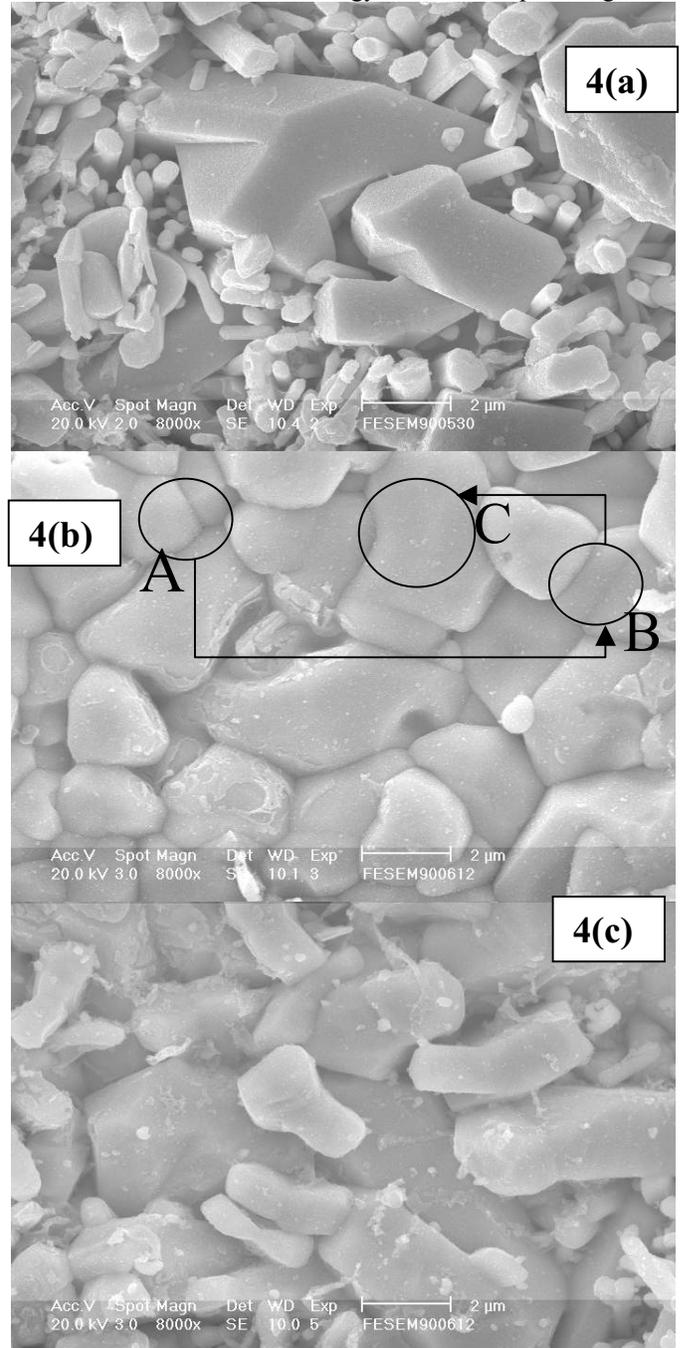


Figure 4 Intermetallic compounds formed at the interface of solder bump (a) as reflowed, (b) after aging at  $150^\circ\text{C}$  for 1000 hours, (c) after humidity test at  $85^\circ\text{C}/85\text{RH}$  for 1000 hours.

behavior also consumes most of the interdiffusing Ni and Sn elements. Thus the increase of the compound layer thickness is restricted during long time testing due to the planar direction growth of the compounds. The growth of the intermetallic compound can be ascribed to two paths. In the beginning of reflow or solid state diffusion, Ni and Sn elements diffuse to the nuclei and results in traditional nucleation and growth behavior. The crystals kept growing

with the aid of coming elements until they encounter each other as denoted in “A” of Figure 4(b). The continuing aging will induce the inter-diffusion between neighboring crystals that starts diminishing the boundary. This is the occurrence from “A” to “B”. Eventually, the crystals grow as depicted by the direction from “B” to “C”. The path from “A” to “C” is actually the “sintering” of crystals.

The interaction forms large crystals at the interface. Cu and Ni could form compound with Sn as long as they are in contact with Sn. The results of XRD analysis, Figures 5(a) and 5(b), however, delineate that the as reflowed solder bump only forms  $\text{Ni}_3\text{Sn}_4$  compound.  $\text{Ni}_3\text{Sn}_4$  remains as the only compound even after 1000 hours of aging or humidity test. This result further indicates the efficacy of the electroless nickel as a diffusion barrier for the solder bump.

**4. Conclusion**

The flux content of the solder paste does not affect the interaction between solder and UBM of flip chip solder bump during reflow. A layer of 5 crystalline electroless nickel deposit is effective as a diffusion barrier for the print solder bump. The intermetallic compound formed between electroless nickel deposit and printed solder bump is  $\text{Ni}_3\text{Sn}_4$ . The growth of the intermetallic compound crystal is ascribed to the diffusion of the constituent elements, Ni and Sn, and the sintering behavior of the crystals.

**Acknowledgments**

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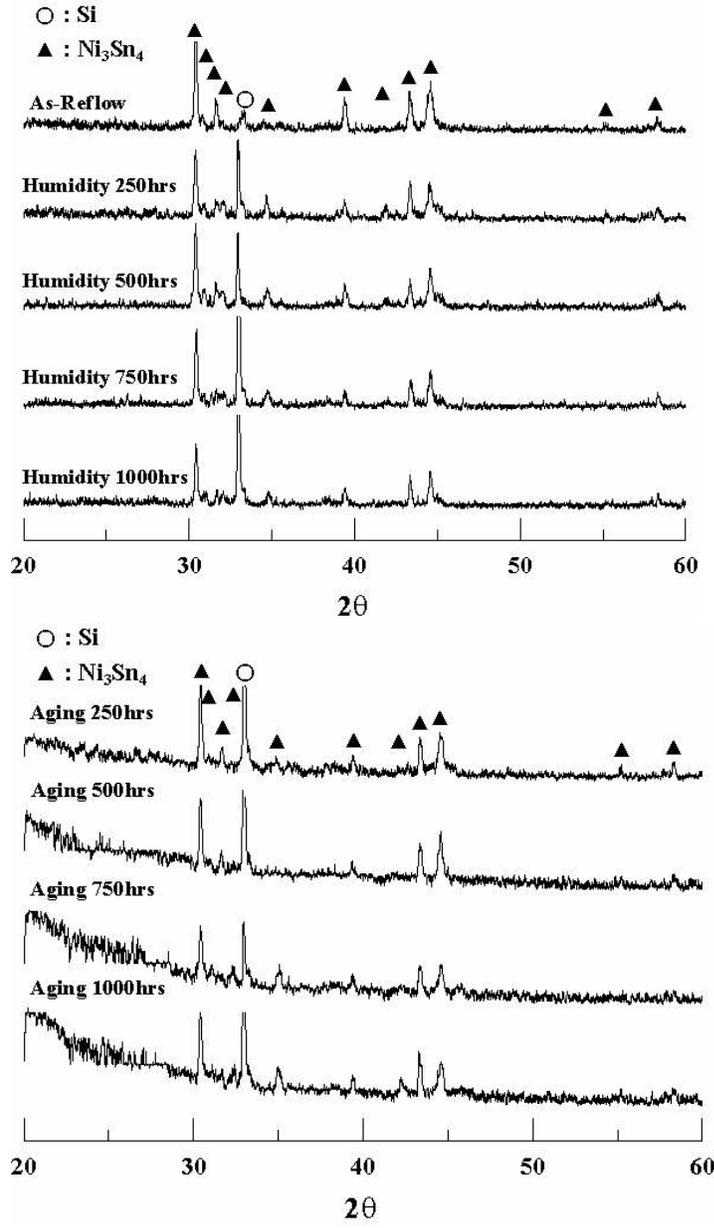


Figure 5 XRD analysis of the intermetallic compounds formed for solder bump (a)as reflowed and humidity tested, (b)aged at 150°C.

# A Study about Solder Bumping Process by using the Electro-plating Method

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## Abstract

Solder bump whose pitch is 150~300  $\mu\text{m}$  was fabricated on Si substrate by electroplating with the medium thickness (~30  $\mu\text{m}$ ) photoresist. TiW/Cu/Cu mini bump was used as a UBM (under bump metallurgy) layer. TiW (0.3  $\mu\text{m}$ )/Cu (0.7  $\mu\text{m}$ ) was deposited by sputtering and Cu mini bump (5~15  $\mu\text{m}$ ) was formed by electroplating. After UBM formation, subsequently, solder bump of mushroom shape was formed by electroplating. In electroplated solder bumping process, the control of the composition is one of the most important key technologies. However, during the formation of a solder mushroom, the composition of solder bump changes due to the variation of plating area. In order to obtain the uniform solder composition with the variance of plating area, applied current was controlled under the consideration of plating area. By controlling the applied current, the composition of solder bump can be controlled within 4%. Solder ball size after reflow could be controlled by calculating the amount of plated solder and measuring the mushroom diameter. The uniformity of mushroom solder bump was 2.63% in chip and 3.69% in wafer before reflow and 1.59% in die and 3.67% in wafer after reflow. The shear strength of solder ball was ~50 MPa and failure mode was inside soft solder shear mode.

## Introduction

Flip chip technology has recently begun to receive a great attention in optoelectronic devices, RF devices and standard integrated circuit (IC) application. Its advantages are low depth profile, shrinkage of size, low assembly cost and high performance. For flip chip technologies, various interconnection materials and methods such as tape-automated bonding, isotropic and anisotropic conductive adhesives, metal bump, compliant bumps and solder bumps have been developed. Among these, solder bumped flip chip is widely used due to low electrical resistivity, high reliability, low cost, self alignment during assembly, and compatibility with surface mounting technology (SMT).

Solder bumping techniques can be divide into three categories depending on the fabrication processes, C4 process, electroplating process and stencil print process. In C4 Process, Cr/CrCu/Cu Under Bump Metallurgy (UBM) has been used and solder is formed by thermal evaporation method. As a solder material high lead solder is used. The minimum pitch in C4 process is 250  $\mu\text{m}$ . C4 process has a long experience so it shows high reliability. However, the bumping cost is expensive. Electroplating process uses TiW/Cu UBM system. Various kinds of solder composition could be achieved by electroplating. One of the great advantage in electroplating

process is that the fine pitch bump can be fabricated. The minimum pitch in electroplating process is 100  $\mu\text{m}$ . The other merit of electroplating process is accommodation to 300 mm wafer with high uniformity. The bumping cost is less expensive than C4 process. In stencil printing, electroless Ni, sputtered NiV or Ni are used as a UBM materials. The minimum pitch in stencil printing process is 150  $\mu\text{m}$ . The merits of stencil printing are it is a low cost bumping process and the composition control is very easy so it has been accepted as a suitable bumping solution in lead free solder. However, it is very difficult to make the uniform bump in a large size wafer.

Recent great advances in semiconductor fabrication technology make it possible to minimize chip size, which results in increasing the number of I/O per unit area. So the demand of high density and fine pitch interconnection technology is continuously growing. Among the solder bump techniques, the electroplating method is most suitable process for the high density and fine pitch solder bump. In electroplating solder bump process, the control of the solder ball size is very important, particularly, in fine pitch solder bump. The solder ball height is a critical factor in flip chip assembly because it directly affects on the solder joint reliability.

In the attachment of IC to a circuit board, the control of the IC-substrate gap is a key factor. The amount of collapse of the solder bump from the pre-assembled condition is controlled by several variables including the solder volume, the size of the pads on IC and substrate, and the size of the IC. Goldman[1] assumed the collapsed solder shape of a solder bump after an IC was attached to a substrate to be that of a truncated sphere with flat faces on the top and bottom corresponding to the IC and substrate pads. The collapse sets the IC-substrate gap distance, which must be wide enough to allow for reliable application of an underfill material into the gap. If the gap is too narrow the underfill material will not completely fill the gap, which can lead to premature failures in the solder joints. Therefore, for any given bump pitch it is desirable to maximize the solder volume to maximize the IC-substrate gap after attach. If it is determined that the IC-substrate gap will be too narrow then dummy bumps or spacer must be used to control the gap width.

As the bump pitch decreases the maximum solder volume that can be deposited onto a bump site on an IC also decreases. While, in a view point of printed circuit board fabrication, the cost of the circuit board which has a small metal pad that are narrow enough to prevent a large collapse during the reaction is high. So it is desirable to be able to predict the maximum solder volume possible for a given pitch and the IC-circuit board gap height after attach. After solder is deposited onto

the input/output (I/O) pads of the IC's on a wafer, the wafer goes through a heating cycle called reflow during which the solder melts, forms a sphere like shape, and finally solidifies. It is one of the purposes of this paper to discuss a model for prediction the final bump shape based on the solder volume, and then to discuss experimental results related to the validation of the model. An adequate model for predicting require solder volumes for given bump pitches can be used with the results from Lin, Patra, and Lee[2] to determine the final gap heights and the feasibility of bump pitch designs.

### Prediction of solder bump height and diameter

The physical model for solder bump consists of a circular metal pad with radius  $R_{UBM}$ , and a specified volume of solder,  $V_s$ , on the metal pad. It is assumed that the solder material reacts with or adheres to the metal pad, and that the base of the solder bump is constrained to have a radius  $R_{UBM}$ . This model is therefore that of a sessile drop. It is also assumed that the dimensions of the solder after solidification are the same compared to the molten solder. This requires that no voids form during solidification and that no shrinkage of the solder occurs during solidification.

One of the important parameters in determining the equilibrium shape of sessile drop is the dimensionless bond number,  $\beta$ , given by  $\beta = (\rho g / \sigma) b^2$  where  $\rho$  is the density of the solder,  $g$  is the acceleration due to gravity,  $\sigma$  is the surface tension, and  $b$  is the radius of curvature at the apex of the droplet. When  $\beta < 0.1$  the expected shape of a droplet is spherical [3]. This situation occurs when  $\rho < 20$  grams/cm<sup>3</sup>,  $\sigma > 50$  dynes/cm, and  $b < 150$   $\mu$ m. This range of solder properties and final solder bump dimensions is more than adequate for application to solder bump technology for flip chip applications. So, for a drop of molten solder on a metal pad, with which the solder reacts or wets, the final solder bump shape can be modeled as a truncated sphere.

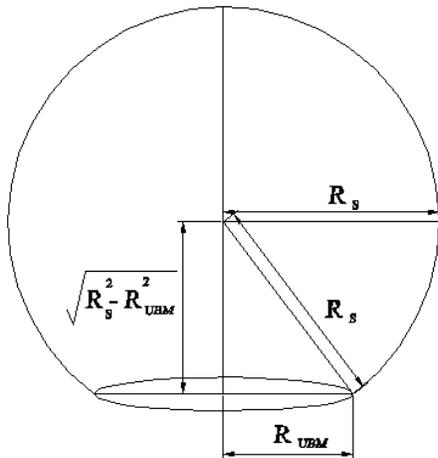


Fig. 1. Schematic diagram of truncated sphere

In order to calculate the solder ball volume, it is assumed that the solder shape after reflow is truncated sphere as shown in Fig. 1. If the radius of solder ball,  $R_s$ , and the radius of UBM open,  $R_{UBM}$ , are known, the volume of solder,  $V_s$ , and

solder ball height,  $R_H$ , after reflow can be calculated by using the eqs. (1) and (2).

$$V_s = \pi \int_{-\sqrt{R_s^2/k^2 - R_{UBM}^2}}^{R_s} \left( \frac{z^2}{k^2} - R_s^2 \right) dz \quad (1)$$

$$R_H = k \sqrt{R_s^2 - R_{UBM}^2} + R_s \quad (2)$$

In fact, solder ball shape is almost identical with a sphere. However, as a solder ball size increase, the solder ball shape changes to ellipsoid. Generally, the diameter is larger than the height. The volume of a ellipcity can be corrected by introducing a  $k$  factor.  $k$  factor mainly depends on the solder size. Its value can be determined by several experimental results. However,  $k$  is fixed with 1 (In sphere,  $k=1$ ) for the simplicity of the calculation.

In order to obtain the adequate solder ball size after reflow, the volume of mushroom has to be calculated. In

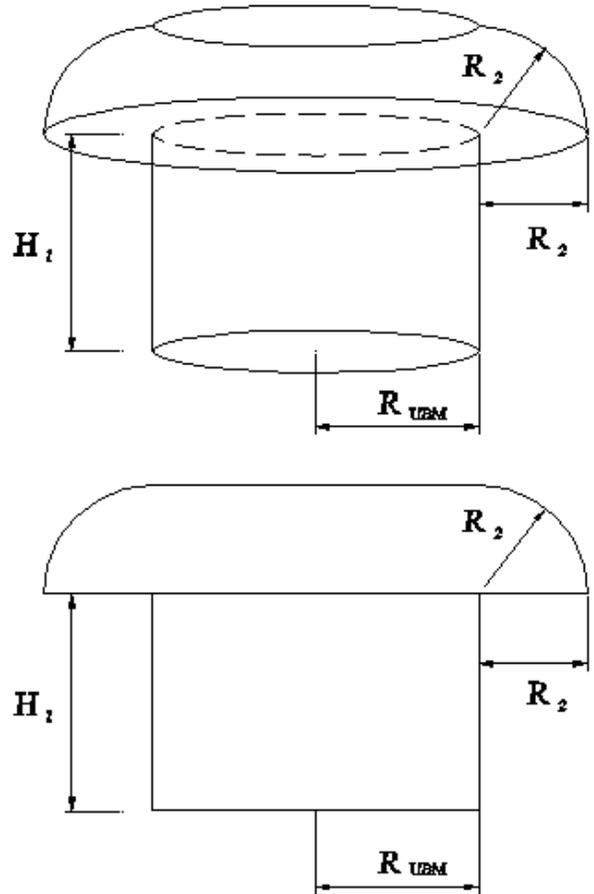


Fig. 2. Schematic diagram of mushroom bump

order to calculate the mushroom volume, it is assumed that mushroom cap grows isotropically. It means that the lateral direction growth rate and the vertical direction growth rate are the same. The mushroom volume can be divide into two parts, mushroom cap portion,  $V_{S1}$ , and cylinder portion,  $V_{S2}$ . The

volume of mushroom cap can be calculated by integrating the eq. (3).

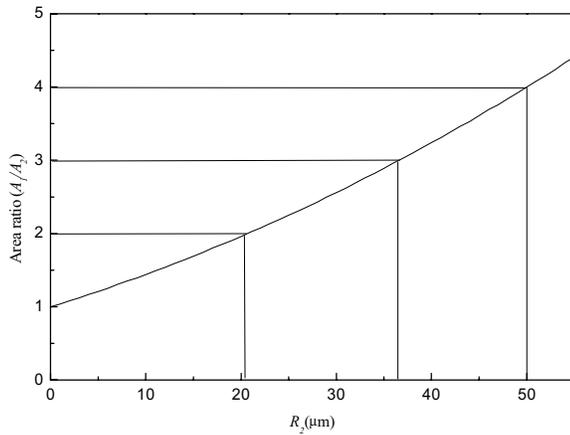
$$V_{S1} = \pi \int_0^{R_2} (R_{UBM} + \sqrt{R_2^2 - Z^2})^2 dz \quad (3)$$

The result of integral is eq (4). The mushroom volume is summation of eqs. (4) and (5).

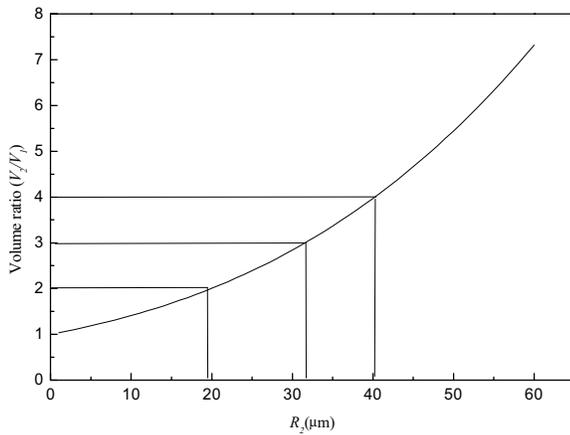
$$V_{S1} = \pi [R_2 R_{UBM}^2 + \pi R_{UBM} R_2^2 / 2 + 2R_2^3 / 3] \quad (4)$$

$$V_{S2} = \pi R_{UBM}^2 \times H_1 \quad (5)$$

$$V_S = V_{S1} + V_{S2} \quad (6)$$



(a)



(b)

Fig. 3. (a) The predicted mushroom surface area ratio to UBM surface area as a function of  $R_2$  (b) The predicted mushroom volume ratio to cylinder volume (the solder volume remain in PR) as a function of  $R_2$  when UBM diameter = 100  $\mu\text{m}$  and PR thickness = 30  $\mu\text{m}$ .

where  $H_1$  is the photoresist (PR) thickness and  $R_2$  is the cap height.

In electroplating, the solder composition can be varied by applied current density. In mushroom plating, the surface area changes depending on  $R_2$ . As  $R_2$  increases, the plating area increases and the current density decreases. In order to correct the current density, the surface area of solder cap has to be calculated. The surface area of solder cap,  $A$ , also divide into two part, a curved area,  $A_1$ , and a flat area,  $A_2$ . The curved surface area of solder cap also calculated by simple integral using eq. (7).

$$A_1 = 2\pi \int_0^{R_2} (R_{UBM} + \sqrt{R_2^2 - Z^2})^2 dz \quad (7)$$

$$A_2 = \pi R_{UBM}^2 \times H_1 \quad (8)$$

$$A = A_1 + A_2 \quad (9)$$

Fig. 3 shows the mushroom surface area and the volume change as a function of  $R_2$ . From the Fig. 3(a), we can figure out that when  $R_2$  is approximately 21  $\mu\text{m}$  the current density drops to the half of its original value. It means that the applied current has to be increased in order to maintain the proper current density. From the Fig. 3(b), we can also figure out that when  $R_2$  is approximately 40  $\mu\text{m}$  the volume of the solder bump is four time larger than that of the solder remained in a via hole. It means that the volume of mushroom solder is equivalent to that of the solder filled in the hole of PR with thickness of 120  $\mu\text{m}$ .

To get the preset solder ball size, the volume of solder ball after reflow has to be calculated using the  $R_{UBM}$ . The volume of mushroom also has to be calculated as a function of  $R_2$ . After choosing  $R_2$  with taking solder volume into consideration, the applied real current density has to be calculated to control the composition of deposited solder. However, since the surface area of mushroom rapidly increases as  $R_2$  increases, it is impossible to control the solder composition with one step plating. To compensate the applied current density, multi step plating is required.

Fig. 4. shows the Sn concentration change as a function of a current density. In order to obtain the eutectic solder, the applied current density should be located between 2 and 7 ASD (Ampere per square decimeter). This available solder plating range is relatively wide than other solder solutions. In each plating step, applied current should be adjusted to keep the real applied current density from escaping the available current density range.

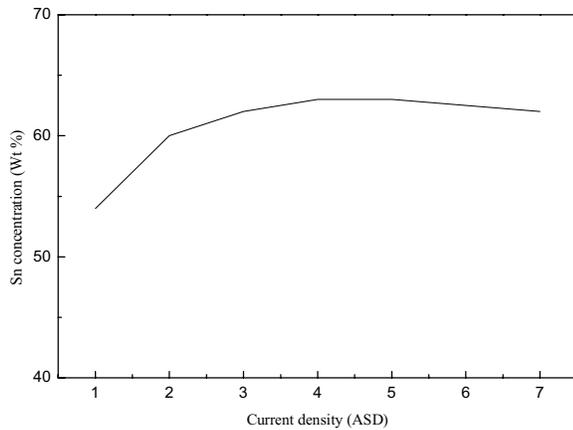


Fig. 4. Sn content change as a function of applied current density. Solder plating conditions are Sn concentration in solution is 69%, flow rate is 20 l/min and working temperature is 20°C.

### Experimental procedures

To verify the validity of the truncated sphere model the samples of solder bumps were prepared on 6 inch Si wafers using an electroplated solder bump process.

Fig. 5. shows the schematic diagram of solder bumping process using electroplating method. Before UBM metal layer deposition, the surface of a wafer was cleaned by RF plasma for removing the contamination and a native oxide layer. After cleaning, TiW layer with thicknesses of 0.3 μm was deposited on the whole Si wafer by RF plasma sputtering. TiW acts as a diffusion barrier and an adhesive layer. Subsequently, Cu seed layer with thickness of 0.7 μm for electroplating was deposited on a TiW layer. The thick photoresist (30 μm) was coated on UBM layer by a spin coater. The mask pattern for lithography process has circular and square openings with sizes of 50~200 μm and with a pitch of 150~300 μm. Photoresist with a thickness of 30 μm has been patterned. The photoresist was exposed and developed. After development, the patterned wafer was slightly etched by RF plasma for removing the residue on metal UBM. For electroplating Cu mini bump, specially designed plating machine was used. The plating bath is very similar with cup type plating machine. However, the wafer could eccentrically rotate for removing the micro-bubble and improving the agitation. Using this machine, Cu mini bump with thickness of 15 μm was electroplated into the holes. Subsequently, the eutectic solder (63Sn/37Pb) was electroplated from an alloy electroplating chemistry with conventional cup type plating machine. To improve the uniformity and rapidly remove the micro-bubble, specially designed anode plate was used. After solder plating, the

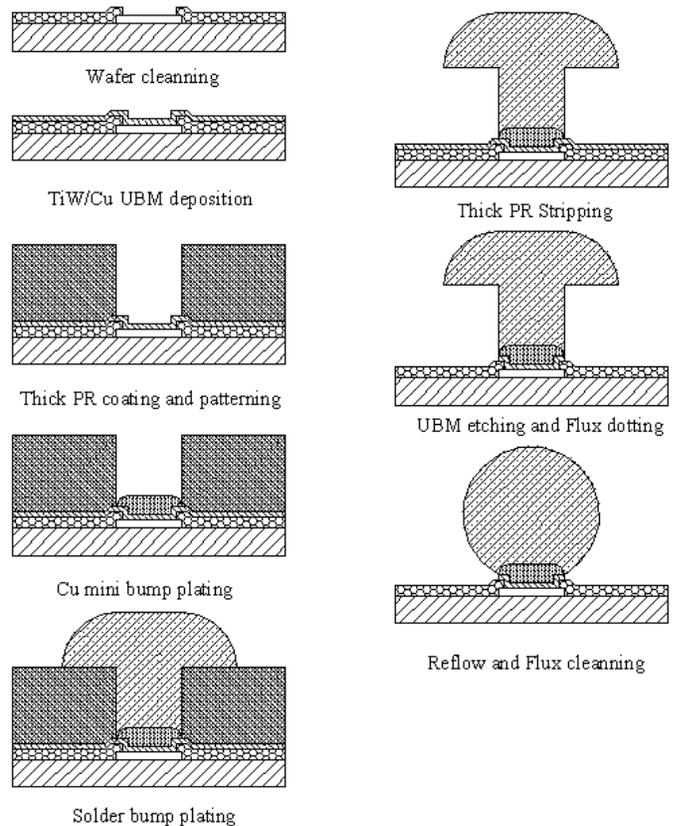


Fig. 5. Schematic diagram of solder bumping process using electroplating method.

photoresist was then removed and the excess sputtered Cu metal and TiW metal etched off the wafer. Finally, flux was dotted on the mushroom solder, then the entire wafer was reflowed.

Height and diameter of solder bump was measured by using the optical microscope. Height measurement was done by focusing on the surface of the wafer and then on the top of the solder bump, measuring the distance between the two focal planes with a digital micrometer that was attached to the focusing mechanism of the microscope. Radius measurements were done using an optical microscope configured with a video and electronics width measurement system. The errors associated with the individual height and radius measurements is ± 0.5 and ± 1.0 μm, respectively. The error ranges are confirmed by SEM measurements. All subsequent calculations are based on these measurements.

Table I. The sizes of solder ball and mushroom solder.

$R_{UBM}$ ( $\mu\text{m}$ )	$R_2^h$ ( $\mu\text{m}$ )	$R_2^r$ ( $\mu\text{m}$ )	$V_2'(\mu\text{m}^3)$	$d_1$ ( $\mu\text{m}$ )	$h_1$ ( $\mu\text{m}$ )	avg $R_2$ ( $\mu\text{m}$ )	$d_2$ ( $\mu\text{m}$ )	$h_2$ ( $\mu\text{m}$ )	$V_2(\mu\text{m}^3)$	$\Delta V$	$D_{mea}$ ( $\mu\text{m}$ )	$H_{mea}$ ( $\mu\text{m}$ )	$\Delta D$	$\Delta H$
25	23.3	26.1	209994	75	65	24.7	75	65	211303	0.16%	70.3	62.4	7%	4%
25	31.2	34.4	326989	87	78	32.8	87	78	327026	0.00%	84.9	78.1	2%	0%
25	38.5	40.6	457354	96	89	39.5	96	86	456205	0.06%	93.1	85.3	3%	4%
25	42.9	45.9	572478	103	96	44.4	103	96	569723	0.12%	106.0	90.1	3%	7%
30	23.7	27.9	284145	83	71	25.8	83	71	288065	0.34%	78.2	65.9	6%	8%
30	32.7	33.5	412111	95	83	33.1	94	83	412359	0.02%	89.5	80.5	6%	3%
30	36.8	39.8	523601	101	91	38.3	101	91	523755	0.01%	98.8	89.5	2%	2%
30	44.3	45.7	699398	110	101	45	111	102	698528	0.03%	107.3	95	3%	6%
40	25.8	27.2	451476	99	79	26.5	99	79	454090	0.14%	92.3	77.5	7%	2%
40	31.5	33.5	583980	107	88	32.5	107	88	587062	0.13%	105.7	87.6	1%	0%
40	35.7	39.7	720376	112	95	37.7	129	104	725599	0.18%	110.7	97.8	1%	3%
40	46.6	46.7	1020015	126	111	46.6	126	111	1020039	0.00%	128.3	101.9	2%	9%
50	22.7	26.7	585605	111	80	24.7	112	81	599969	0.61%	105.5	79.3	5%	1%
50	29.3	32.4	752675	118	91	30.8	118	91	762516	0.32%	116.1	88.1	2%	3%
50	33.7	39.9	932739	125	100	36.8	126	101	951470	0.50%	121.7	102.6	3%	3%
50	42.6	45.1	1214060	136	114	43.8	135	112	1219377	0.11%	135.7	108.8	0%	5%
60	25	27.6	849317	129	89	26.3	129	89	862736	0.39%	120.0	85.5	8%	4%
60	29.7	32.2	1005961	133	96	30.9	133	96	1018159	0.30%	133.1	97.8	0%	2%
60	31.6	40.9	1173200	139	104	36.2	104	105	1221252	1.00%	135.5	108.7	3%	4%
60	45.5	45.7	1651766	152	122	45.6	152	122	1652465	0.01%	152.3	114.7	0%	6%
75	25.6	28.1	1264691	154	94	26.8	154	94	1285566	0.41%	153.7	89	0%	6%
75	32.8	35.6	1602619	160	107	34.2	160	107	1624803	0.34%	160.9	104.4	1%	2%
75	36.8	43.6	1894454	165	117	40.2	166	118	1948369	0.70%	159.1	120.3	4%	3%
75	46.9	47.7	2384123	175	132	47.3	175	132	2389393	0.06%	173.8	126.6	1%	4%
												average	3%	4%

### Results and Discussion

Results of the solder bumps measured by optical microscope are shown in Table I. In Table 1,  $R_2$  is one of the most important factors in calculating the solder volume, height and diameter. So exact measurement of  $R_2$  is important to compare the simulation results to measured results. The solder bump  $R_2$  was measured in the following two ways: 1) measuring the bump heights and 2) measuring the bump radii and subtracting  $R_{UBM}$ . The two values of  $R_2$  determined by measuring the height and the radii will be referred to as  $R_2^h$  and  $R_2^r$ . Measuring  $R_2$  using the two methods described provides data on the validity of assumption that the electroplating rate is equal for the lateral and vertical growth of the cap portion of the bump. However,  $R_2^h$  is not equal to  $R_2^r$ . As shown in Table I,  $R_2^r$  is slightly larger than  $R_2^h$ . It does not mean that the above assumption is not valid. The main reason of the difference between  $R_2^r$  and  $R_2^h$  is due to an enlargement of the upper diameter of via hole by plasma etching process. In photo process using thick photoresist, plasma etching process is inevitable to remove the residue. During plasma etching process, the energetic plasma particles bombard the surface of photoresist resulting in rounding the corner of PR as shown in Fig. 6. It widens the upper diameter of via hole by 1~2  $\mu\text{m}$  as shown in Fig. 6. It means that, initially,  $R_2^r$  is larger than  $R_2^h$  by 1~2  $\mu\text{m}$  and this affects the final values of

$R_2^r$  and  $R_2^h$ . In order to calculate the volume of mushroom using eq. (5), average  $R_2$  is obtained by averaging the values of  $R_2^r$  and  $R_2^h$ . The calculated mushroom volume,  $V_s$ , using average  $R_2$  is represented in Table I. For more exact calculation, the volume of mushroom,  $V_s'$ , depending on  $R_2^r$  and  $R_2^h$  is also calculated. In order to calculating  $V_s'$ , eq. (5) should be modified. By taking  $R_2^r$  and  $R_2^h$  into consideration, eq. (3) can be modified as following equation.

$$V_{s1}' = \pi \int_0^{R_2^h} \left( R_{UBM} + \frac{1}{R_2^h} \sqrt{R_2^{h2} R_2^{r2} - R_2^{r2} Z^2} \right)^2 dz \quad (10)$$

By simple mathematical integral, eq. (11) can be derived.

$$V_{s1}' = \pi [R_2^h R_{UBM}^2 + \pi R_{UBM} R_2^h R_2^r / 2 + 2 R_2^{h2} R_2^{r2} / 3] \quad (11)$$

Using eq. (11) and eq. (6),  $V_s'$  can be calculated and is represented in Table I. The calculation values of  $V_s$  is not much different with those of  $V_s'$ . It means that the solder volume calculated using eqs. (3)~(6) is valid.

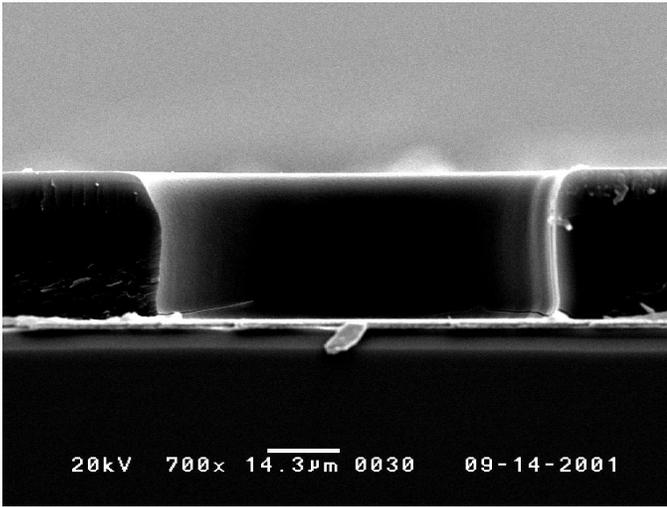
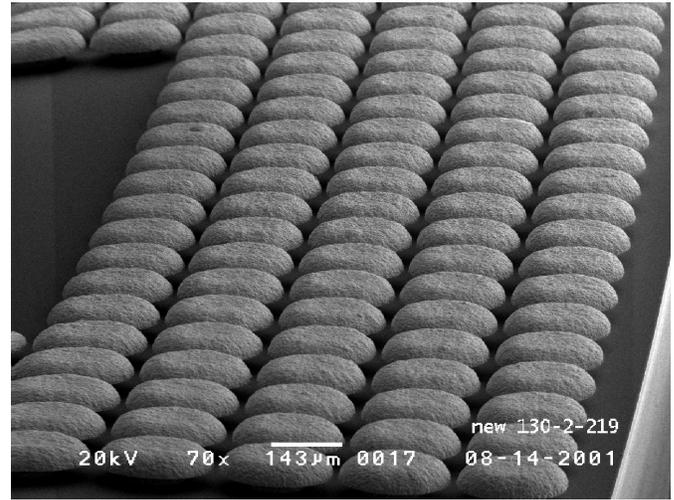


Fig. 6. SEM images of via hole after desccum.

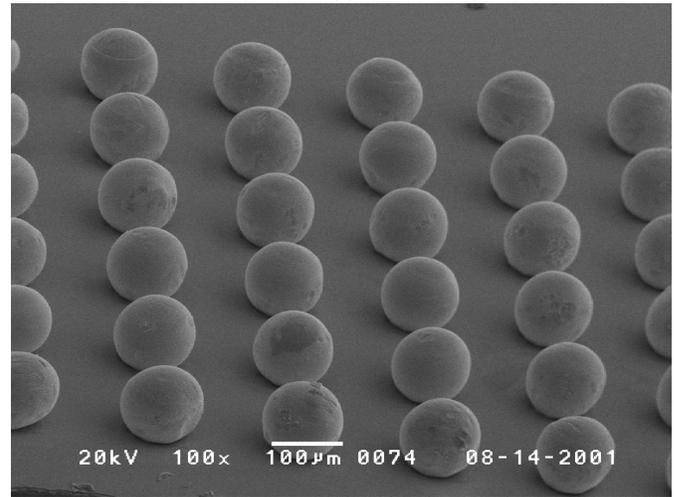
By using the mushroom volume ( $V_s$  or  $V_s'$ ), eq. (1) and eq. (2), the solder ball diameter ( $d_1$ , or  $d_2$ ) and height ( $h_1$ , or  $h_2$ ) after reflow can be calculated. The calculated solder ball sizes and the measured solder ball sizes are also represented in Table I. In Table I,  $\Delta V$  is the volume difference between  $V_s$  and  $V_s'$ .  $\Delta D$  and  $\Delta H$  are difference between calculated values and measured values in diameter and height, respectively. Both the height and the radius experimental results showed good correlation to the calculated results. For the final solder bump heights the average discrepancy between the experimental and theoretical results is 4% with the maximum difference being 9%. For the final solder bump radii the average discrepancy between the experimental and theoretical results is 3% with the maximum difference being 8%. The possible sources of error are ignorance of the volume of round corner of PR, the angle of PR wall, and the actual shape of solder ball as well as the measurement error.

The available solder ball sizes are mainly restricted by a given bump to bump pitch among the various parameters. Particularly, for fine pitch and high density applications, it is very important to predict the solder ball height and radius after reflow. Because the solder ball height is a critical factor in flip chip assembly, as previously mentioned.

Fig. 7 shows SEM images of (a) a mushroom shape solder bump array and (b) a solder ball array after reflow fabricated using PR with thickness of  $30\ \mu\text{m}$ . As shown in Fig. 7(a), the gap between mushroom caps should be tightly controlled in order to obtain the maximum ball height at a given pitch and a given UBM opening. In order to conduct the whole process including PR strip and UBM etching and to avoid the bridging during the solder plating, minimum gap distance should be larger than  $10\ \mu\text{m}$ . Table II shows the available maximum solder ball size depending on the pad pitch and the UBM size when PR with thickness of  $30\ \mu\text{m}$  is used.



(a)



(b)

Fig. 7. SEM images of (a) a mushroom shape solder bump array and (b) a solder ball array after reflow fabricated using  $30\ \mu\text{m}$  medium thickness PR.

Table II shows that to obtain the maximum solder ball height at a given bump to bump pitch, small size UBM is advantageous. However, since the UBM area (solder wetting area) is directly connected to the shear value, the proper UBM area should be established for reliability. The uniformity of solder bump is also measured by optical microscope. Table III shows the measurement results of uniformity. Five chips are selected in a wafer (center, top, bottom, right side and middle point between center and right side). In each chips, four point (top, right, left, bottom) bumps are measured. The uniformity is calculated using the following equation.

$$\text{Uniformity} = (\max - \min) / (\max + \min) \times 100 \quad (12)$$

Table II. Available maximum solder ball sizes depending on the pad pitch and the UBM size when PR with thickness of 30  $\mu\text{m}$  is used

Pad Pitch[ $\mu\text{m}$ ]	UBM Size[ $\mu\text{m}$ ]	Max. ball height[ $\mu\text{m}$ ]
150	50	91
150	70	86
180	60	95
180	80	93
180	100	84
180	120	78
200	60	118
200	80	110
200	100	106
200	120	90
220	60	126
220	80	116
220	100	114
220	120	106
250	80	141
250	100	133
250	120	120
250	150	118
300	80	170
300	100	164
300	120	152
300	150	145

The composition of solder bump was examined by Energy Dispersive X-ray Analysis (EDAX) and Auger electron spectroscopy (AES). Table III shows the composition of mushroom solder bump by using EDAX. Eutactic solder composition can be obtained using multi-step plating by controlling the applied current density within 4-6 ASD region under the consideration of the change of mushroom surface. The EDAX results are confirmed by Auger analysis which shows maximum 4% deviation from the results of EDAX.

Table III. Composition analysis results of mushroom solder bump by EDAX

	Element	Line	Weight %	Error	Deconvolution Regions
Multi step (1-4 ASD)	Sn	L $\alpha$	55.9	0.227	3.160-3.760
	Pb	M $\alpha$	44.1	0.181	2.090-2.630
Multi step (4-6 ASD)	Sn	L $\alpha$	62.0	0.432	3.170-3.750
	Pb	M $\alpha$	38.0	0.301	2.090-2.620
One step (2 ASD)	Sn	L $\alpha$	50.9	0.465	3.140-3.800
	Pb	M $\alpha$	49.1	0.265	2.080-2.650
One step (5 ASD)	Sn	L $\alpha$	52.8	0.513	3.140-3.790
	Pb	M $\alpha$	47.2	0.296	2.070-2.650

Table IV. Uniformity measurement results of solder bump.

		Position within chip					Uniformity within chip
		Top	Right	Bott.	Left	Avg.	
Before reflow, mushroom height, UBM diameter = 90 $\mu\text{m}$							
Position within wafer	Top	35.8	35.8	36.4	36.1	36.03	0.83%
	Cen	36.4	36	37.2	37.7	36.83	2.31%
	Bott	37	37.4	37.2	37.2	37.2	0.54%
	Side	36.9	37.1	36.5	35.2	36.43	2.63%
	Mid	37.9	36.4	37.5	36.9	37.17	2.02%
Uniformity in wafer 3.69%							
Before reflow, mushroom diameter, UBM diameter = 90 $\mu\text{m}$							
Position within wafer	Top	119.8	119.9	121	119.9	120	0.29%
	Cen	122.4	123.1	124	124.4	123.4	0.81%
	Bott	120.3	121.2	120	119.9	120.4	0.54%
	Side	119	119.3	120	119.9	119.4	0.38%
	Mid	121.7	121.9	123	121.5	121.9	0.45%
Uniformity in wafer 2.22%							
After reflow, solder ball height, UBM diameter = 90 $\mu\text{m}$							
Position within wafer	Top	84.7	83.2	83.2	83.4	83.625	0.89%
	Cen	84	83.9	84.5	86.6	84.75	1.58%
	Bott	85	87.2	87.5	84.9	86.15	1.51%
	Side	83.9	82.4	81.3	82.6	82.55	1.57%
	Mid	82.8	84.5	82.5	83.2	83.25	1.20%
Uniformity in wafer 3.67%							
After reflow, solder ball diameter, UBM diameter = 90 $\mu\text{m}$							
Position within wafer	Top	104.7	103.7	106	103.2	104.4	1.24%
	Cen	107.5	107.8	108	108.2	107.9	0.32%
	Bott	105.1	105.5	105	107.6	105.9	1.18%
	Side	102.4	105	104	105.7	104.3	1.59%
	Mid	108.4	107.4	108	105.3	107.4	1.45%
Uniformity in wafer 2.85%							

The uniformity of mushroom height is 2.31% within chip and 3.69% within wafer and that of mushroom diameter is 0.81% within chip and 2.22% within wafer. After reflow, The uniformity of solder ball height is 1.58% within chip and 3.67% within wafer and that of solder ball diameter is 1.59% within chip and 2.85% within wafer. By the several measurements of uniformity to the different bump which has different UBM size, we can confirm that the solder bump can be controlled within 3% in die and within 5% in wafer before reflow and after reflow.

### Conclusions

In this study, the equilibrium shapes of reflowed solder ball were modeled as truncated spheres based upon capillary physics. Experimental results show that the truncated sphere model can be applied to the solder ball whose size is 70~170  $\mu\text{m}$ . By calculating the mushroom volume, the solder ball radii and heights are predicted within an average of 4% with a maximum difference of 9% and within an average of 3% with

a maximum difference of 8%. The composition of solder bump can be controlled within  $\pm 4\%$  by using a step plating method under the consideration of mushroom surface area. Finally, the uniformity of solder bump can be controlled within 3% in chip and 5% in wafer before reflow and after reflow.

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