

Session FC-1

Flip Chip(1)

Cu Bump Interconnections in 20 μ m Pitch Utilizing Electroless Tin-Cap on 3D Stacked LSI

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Cu Bump Interconnections in 20μm pitch utilizing Electroless Tin-Cap on 3D Stacked LSI

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Abstract

The electroless tin-plating on copper has the preferable characteristic for the thermal compression bonding, although it is easy to decrease in thickness by the heating at the bonding because of the diffusion with copper. Therefore, the bonding temperature profile was determined to have the lower pre-heating to evaluate the bondabilities with the copper-bumps in 20μm pitch dressed thin tin-caps on each bump. As the result, the possibilities of the interconnections in 20μm pitch were confirmed. The bonding temperature was 300°C and the bonding force was 24.5N.

Then, the tin-cap on through-hole electrode (T-COTE) was performed in the electroless plating and the basic bonding condition was evaluated on the vertical interconnections. The results showed the sufficient joint between the Cu electrodes through Si die and the adjacent copper bumps on interposer.

Finally, the results of the feasibilities on the micro-joint at 150°C will be discussed in this paper.

Introduction

Recently, the demand for the high-speed electronics component is quite general for the consumer information equipment. One of the substantial technologies for the high performance is the hyperfine interconnection of the microelectrode [1]. 3D LSI is under developing for a solution to the requirement. Figure 1 shows the 3D LSI structure with the through-hole copper electrodes in the Si devices, which are formed by the reactive ion etching (RIE) process in 20μm pitch for the vertical wiring retributions [2]. Figure 2 shows the interconnection between the opposed copper electrodes with the electroless tin-caps. The high-precision flip-chip bonding technologies in 20μm pitch are applied to connect the copper electrodes through Si devices with the micro-bump formed on each copper electrode to realize the small and high performance 3D LSI [3].

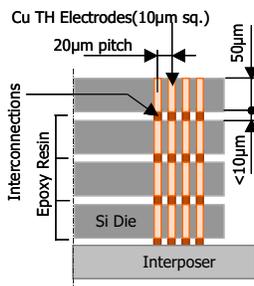


Figure 1 3D LSI Structure

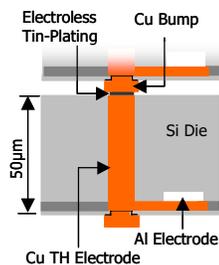


Figure 2 Cu TH Electrode Interconnections

As for the advanced bonding process at the low-profile bonding to take the advantages over conventional technologies, the copper bump bonding process is under development to be applied in the simple interconnections of the through-hole electrodes with the thin metal-caps with a small deformation of the bumps.

In this paper, the results of the studies in the following are discussed in session order.

- 1) The characteristics of the electroless tin-plating on copper.
- 2) The flip-chip bonding evaluation with the tin-capped copper bumps in 20μm pitch.
- 3) Confirmation of the vertical interconnections between the copper electrodes through Si die and the adjacent copper bumps on the interposer in 20μm pitch.
- 4) Feasibilities on the micro-joint in solid-phase as lower temperature at 150°C with tin-plating on copper.

The Characteristics of Electroless Tin-plating on Copper

-Experimental Model

Figure 3 shows the cross-sectional structure of the Si chips applied to the evaluations. They are completely plated with the electrolysis copper plating on the barrier metals. The die size was 10mm square and 625μm in thickness. The thick copper layer in 5μm was formed by electroplating onto the sputtered film consisted with Cu (300nm) and Ti (170nm).

In this evaluation, the electroless plating liquid using the substitution reaction was applied. The reaction is shown in the next equation.

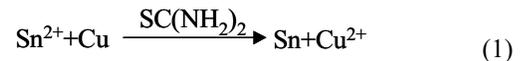


Table 1 shows the plating procedure and the condition in the evaluations. This condition was set to perform the tin-layer on the copper from 0.5μm to 1.0μm in thickness to achieve the thin and the uniform inter metallic compound (IMC) at the bump interconnections.



Figure 3 Si Chip for Evaluation of Tin-Plating

Table 1 Condition of Electroless Tin-plating

	Procedure	Material	Condition
1	Degreasing	Acid	25°C, 2min
2	Activation	Sulfuric Acid	25°C, 2min
3	Tin plating	Plating Liquid	50°C, 15min
4	Cleaning	Alcohol	-

-Tin-Plating Diffusion between Copper Layers

First, the diffusion between the tin-plating and copper layer was analyzed by scanning electron microscope (SEM) and Electron Probe Micro Analyzer (EPMA). Figure 4 shows the results. Just after the tin-plating, there was the tin-layer on the copper layer, although the some reactive layer was found between tin and copper. In addition, after the heating on the plate at 150°C in 5 minutes, there were 2-layered IMC on copper leaving the minute pure-tin-layer.

Commonly, the tin-layer is diffused rapidly with the copper in a short time [4], and the IMC layers formed between the copper and the tin was found as $\eta\text{-Cu}_6\text{Sn}_5$ and $\epsilon\text{-Cu}_3\text{Sn}$ from the atomic weight of each layer [5]. Then, it was analyzed that the detailed characteristics of the initial tin-plating and the diffusion development, especially in case of the electroless plating on copper.

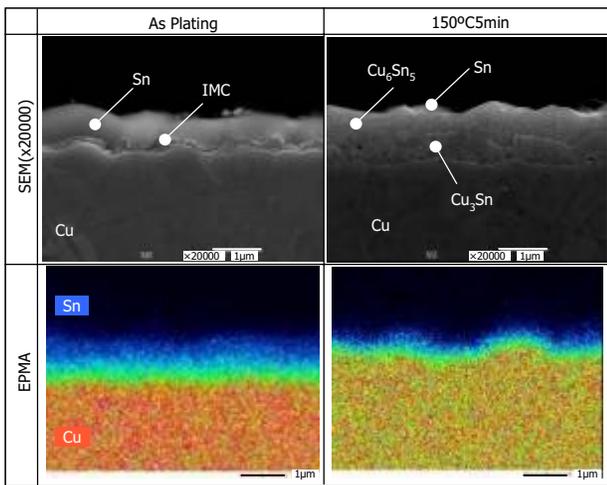


Figure 4 Cross Sections of Tin-Plating on Copper

-Characteristics of Initial Tin-Plating on Copper

Figure 5 shows the results of the X-ray diffraction (XRD) from the surface direction of the initial tin-plating.

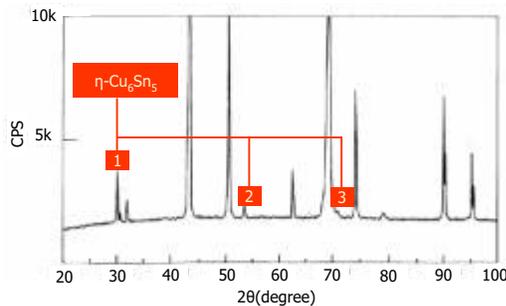


Figure 5 XRD Analysis of Initial Tin-Plating on Copper

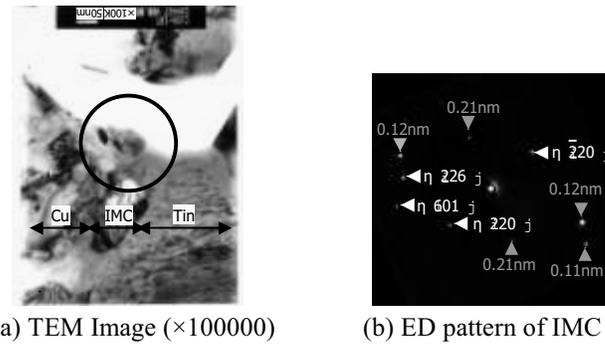
Table 2 shows the results of the identification of each peak analyzed by XRD utilizing the join committee on powder diffraction standards (JCPDS). The results show the existence of $\eta\text{-Cu}_6\text{Sn}_5$ between the electroless tin-plating and the copper layer in the first place.

Table 2 Identification of XRD Analysis of Initial Tin-Plating

No	2θ(deg.)	JCPDS					
		$\eta\text{-Cu}_6\text{Sn}_5$			$\epsilon\text{-Cu}_3\text{Sn}$		
		d (nm)	d (nm)	h k l	d (nm)	h k l	
1	30.17	0.296	0.296	1 0 1	-	-	
2	53.48	0.171	0.171	4 0 2	-	-	
3	70.93	0.133	0.132	2 2 6	-	-	

To confirm the existence of the $\eta\text{-Cu}_6\text{Sn}_5$ in the initial electroless tin-plating, the transmission electron microscope (TEM) and electron diffraction (ED) method were applied to the more detailed analysis. The results are indicated in Figure 6. Figure 6 (a) shows the image of TEM, and (b) shows the results of ED focused at the circle in TEM image.

From the both results shown in the figure, the existence of IMC layer as $\eta\text{-Cu}_6\text{Sn}_5$ formed at tin-plating was proved.



(a) TEM Image (x100000) (b) ED pattern of IMC

Figure 6 TEM and ED Analysis of Initial Tin-Plating

Then the crystal orientation on the most surface of the tin-plating was analyzed by the electron backscatter diffraction pattern (EBSP) [6]. Figure 7 shows the results that compared the crystal orientation of the surface of the copper before electroless tin-plating and the surface after tin-plating. The orientation image microscopy (OIM) map data and inverse pole figures (IPF) indicated that the tin-surface had the intensive orientation at (001) face in the surface axis, while the copper surface had no definite orientation. Moreover, it also suggested that the electroless tin-plating has no compliance with the copper surface due to the low melting point of tin, meanwhile generally the plating metal shows the epitaxial growth [7].

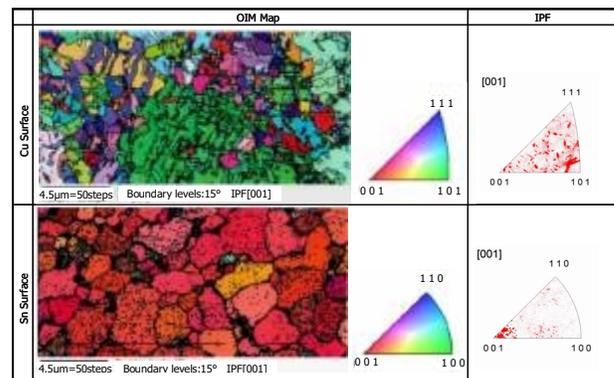


Figure 7 EBSP Analyses of Tin and Copper Surface

-Activation Energy of E-less Tin-Plating Diffusion to Copper

Then, the diffusion characteristics between electroless tin-plating and the copper substrate were evaluated. The sequential electrochemical reduction analysis (SERA) method was applied to the evaluation [8].

The relationship between the thickness of IMC and aging times is expressed in the equation [9]

$$d=(Dt)^{1/2} \tag{2}$$

where d is thickness of the layer, D is the interdiffusion coefficient, and t is the aging time. And the activation energy is given in the Arrhenius equation [9]

$$D=D_0 \exp^{-Q/kT} \tag{3}$$

where D_0 is the interdiffusional constant, Q is the activation energy, k is the Boltzmann constant, and T is the absolute temperature. Each sample was heated on the plate at 120°C, 150°C, and 180°C respectively and the thickness of remained pure-tin-layer was measured by SERA. Figure 8 shows the result of the measurement. From the results, the Arrhenius curve was plotted. Figure 9 shows the plot as in D against $1/T$. As the result, the activation energy, namely Q , for growth of IMC at interface between the electroless tin-plating and the copper substrate, was calculated as 0.90eV. The tendency in the growth and the activation energy were similar to the IMC in the annealed surface mount solder joint [9]. In case that the electroless tin-plating, there was the IMC such as η -Cu₆Sn₅ before aging previously as mentioned above.

Therefore, in the diffusion characteristic between the pure-tin-layer and the copper substrate at low temperature and in short time, it was considered the diffusion between η -Cu₆Sn₅ and the pure-tin was dominant.

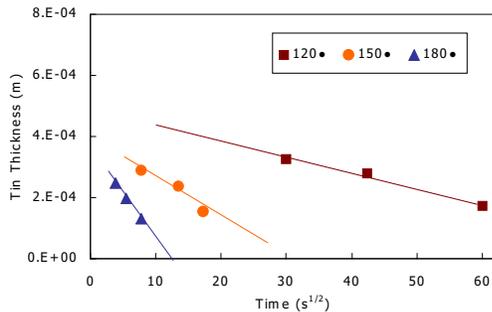


Figure 8 Measurement of Pure-Tin Thickness by SERA

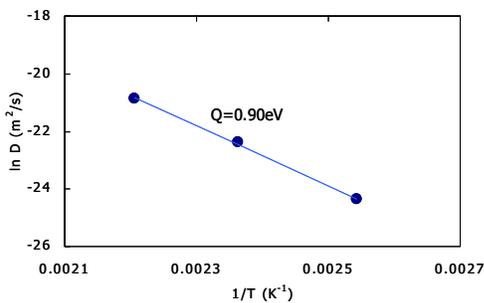
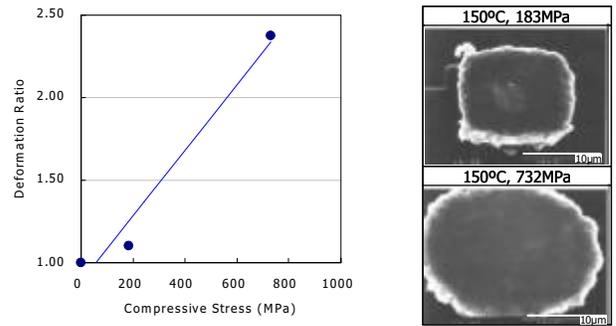


Figure 9 Arrhenius Plot for Growth of IMC at Electroless Tin Plating on Copper

-Hardness and Roughness of Tin-Plating Layer

For the hyperfine interconnections in 20μm pitch, it is important to control the whole deformation of the bumps to keep off the short circuit [10]. Figure 10 shows the impact of the deformation of the copper microbumps in 12μm square at 150°C. Figure 10 (a) indicates the relationship between the bonding pressure and the whole deformation of the Cu bumps in size, and Figure 10 (b) describes the SEM micrographs after the deformation at each pressure. The deformation ration was calculated from the projected area proportion between the deformed bump and the initial bump. As shown in the figure, at the thermal compression bonding, the microbumps are easy to be deformed leading to the fear the electrical defects even at the low temperature and the pressure.



(a) Relationship between Bonding Pressure vs. Bump Deformation (b) SEM micrographs of deformed Cu Bumps

Figure 10 Deformation of Pressurized Cu Bump at 150°C

The tin-plating on the copper bumps is expected to decrease the hardness of the surface at the bonding interface, which contribute to the local deformation to achieve the sufficient interconnections [11]. The nano-indentation is one of the methods to evaluate the mechanical characteristics of the thin metal layer with the control of the micro indenter in nano-meter scale [12].

Figure 11 shows the graphs describing the relationships between the compressing force and the penetration of the indenter measured by the nano-indentation at room temperature. The triangular pyramid indenter with the apex angle at 115° was applied to the measurement and the maximum force at compression was 3mN. The copper surface, the tin-plating surface before aging, and that after the aging at 150°C in 5 minutes were measured. It indicated the tendency to have the large deformation at the indentation in sequence.

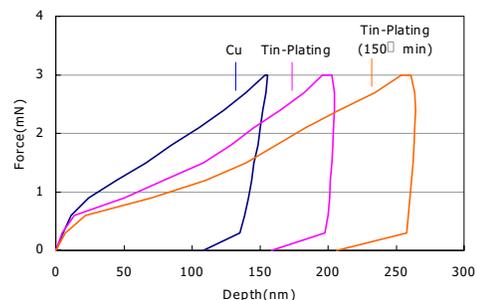


Figure 11 P-h diagram by Nano Indentation

Figure 12 shows the results of the inspections after indentation utilizing atom force microscope (AFM). The definite traces of the indentation were also observed at the tin-plating surface rather than the copper surface, and the largest deformation at the indentation was seen after the aging.

In the same time, the roughness of the surface was changed from the copper surface to the tin-plating surface and the tin-plating surface after aging.

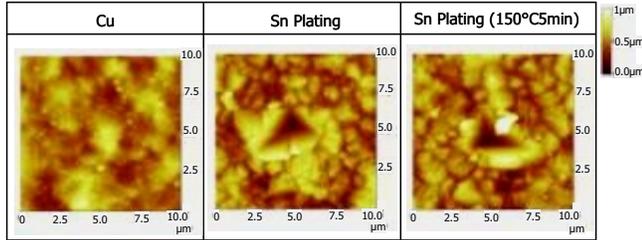


Figure 12 AFM Inspections after Nano-Indentation

The hardness is calculated from the plot in equation [13]

$$H = P_{\max} / \eta k h_{\max}^2 \quad (4)$$

where H is the calculated hardness by nano-indentation, P_{\max} is the maximum form at the measurement, h_{\max} is the maximum indent at the measurement, and η , k are the dimensional coefficient at the calculation.

Figure 13 shows the hardness calculated by nano-indentation and the roughness measured by AFM. As shown in the results, the hardness of the most surface of the bumps was softened with the thin tin-cap formed on the copper. The hardness decreased after aging, but also roughness of the surface increased. In addition, the low hardness after aging is possible to be deformed so large that invites the electrical defect at the thermal compression bonding at the high temperature. Because, the pure-tin was almost disappears and the IMC layers with high-melting point were remained at the bonding interface that could not decrease the whole deformation of the bumps by melting.

From the results of the studies mentioned above, the basic bonding profile was determined to have the lower pre-heating with the copper-bumps in 20μm pitch to evaluate the bondabilities with thin-tin caps. The conditions were set to control the diffusion between the tin and the copper layer before bonding, to keep the softened surface and release the bump deformation by melting, and also to decrease the effects of the roughness at the bonding interface.

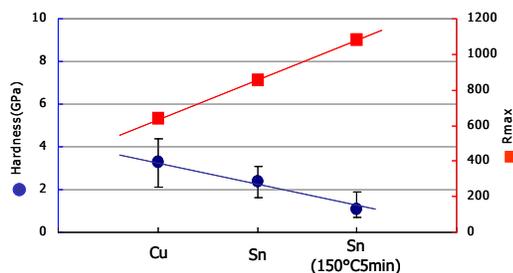


Figure 13 Hardness and Roughness of Tin-Plating

FC Bonding in 20μm pitch with Tin –capped Cu Bumps

-Experimental Model

Then, the flip-chip bondability with the tin-capped copper bumps in 20μm pitch was evaluated on the basic bonding profile. Figure 14 shows the structure for the experiment.

The die and the interposer size were 10mm and 18mm square. The thickness of them was 500μm. Both of the die and the interposer have the aluminum pads to locate the bumps covered by SiN film around the pads as the passivation in 800nm thickness. The 1844 copper bumps were located in 20μm pitch and 5μm in the height peripherally on both of the die and interposer in correspondent. They are connected onto the pads through the under bump metals (UBM), which is constructed with Cu (300nm) and Ti (170nm). Moreover, the electroless tin-cap was performed on each Cu bump in from 0.5μm to 1.0μm thickness.

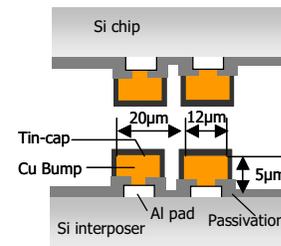
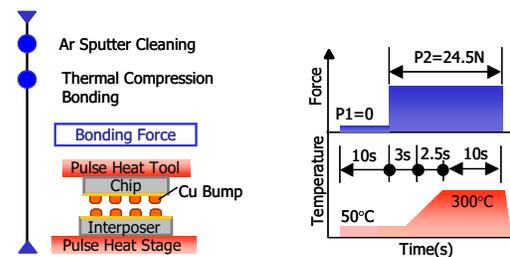


Figure 14 Cu Bumps in 20μm pitch for FC Evaluations

-Experimental Flip-chip Bonding Profile

Figure 15 shows the bonding profile. Figure 15(a) indicates the bonding flow and Figure 15(b) describes the bonding temperature and the pressure applied to the evaluations.

The bonding temperature was set at 300°C to raise the temperature up to the melting point of tin at 232°C to have the liquid-phase diffusion bonding in this evaluation. The bonding force was determined at 24.5N to keep the deformation as mentioned in Figure 10 within 10% as a provisional indication.



(a) FC Bonding Flow (b) Bonding Temp. and Force

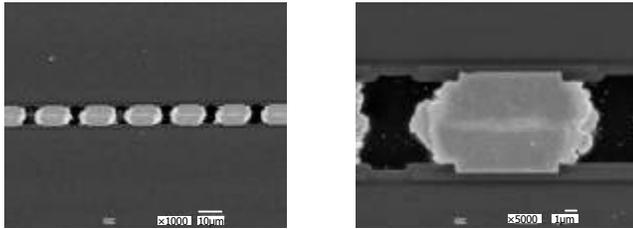
Figure 15 20μm pitch Cu Bump Bonding Profile

First, the bumps were compressed under a low temperature at 50°C. In addition, the both temperatures at the tool and the stage start to rise by the pulse-heat. Then, the temperature rises up to 300°C in around 2.5 seconds at the tool temperature. It was considered that the profile could prevent the disappearance of the pure tin-layer due to the heating up

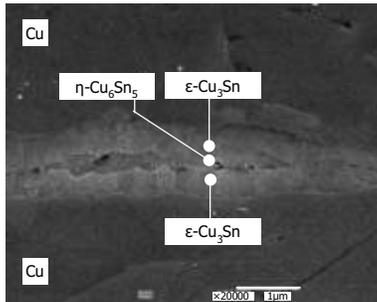
before the bonding. The argon sputter cleaning was performed before the bonding. The bonding time in 10s was constant in this evaluation.

-Results of Copper Bump Bonding in 20μm pitch

First, the bondabilities were confirmed in the cross section by SEM. Figure 16 shows the SEM micrographs. Figure 16(a) focused at the adjacent Cu bumps connected in 20μm pitch. Figure 16(b) magnified one of the interconnections between the Cu bumps. Figure 16(c) was focused on the IMC layers at the interface between the copper bumps.



(a) Cu Bump Interconnections in 20μm pitch (b) Magnified Cu Bump Interconnections

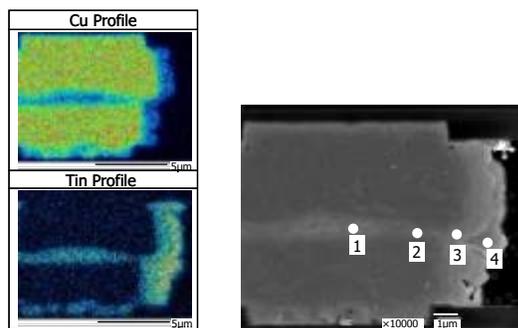


(c) 2-layered IMC between Cu Bumps

Figure 16 SEM Micrographs of Cu Interconnections (300°C)

As shown in the micrographs, it was confirmed that the sufficient interconnections in 20μm pitch and the existence of 2-layered IMC at the interconnections between the copper bumps.

Then, the IMC layer was analyzed by energy dispersive X-ray spectroscopy (EDS). Figure 17(a) shows the results of EDS mapping for the both profile of tin and copper on the area shown in Figure 17(b).



(a) EDS Mapping Data (b) EDS Analysis Points

Figure 17 EDS Analysis at Interconnection (300°C)

Table 3 shows the results analyzed by EDS on each point from No.1 to No.4 indicated in Figure 17(b) to identify the IMC material from the atomic percentage of the elements. As shown in the results, the IMC layer was confirmed that the 2-layered structures consist of η-Cu₆Sn₅ and ε-Cu₃Sn. Moreover, It was found that the extruded pure-tin parts were remained around the bump.

Therefore, the interconnection in 20μm pitch was confirmed at the determined bonding conditions from the characteristics of electroless tin-plating. The optimization of the tin thickness will be the subject in future.

Table 3 EDS Analysis at IMC (300°C)

Temp.	μ	300			
Point	-	1	2	3	4
Cu (at%)	-	65.7	80.0	51.3	0.0
Sn (at%)	-	34.3	20.0	48.7	100.0
Material	-	Cu ₆ Sn ₅	Cu ₃ Sn	Cu ₆ Sn ₅	Sn

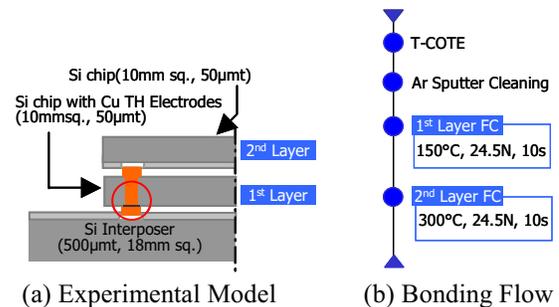
Vertical Interconnections of Cu Electrodes in 20μm pitch

-Experimental Model and Bonding Profile

Next, the possibilities of the vertical interconnections in 20μm pitch between the copper electrodes through Si die and the copper bumps formed on the interposer was confirmed. Figure 18 shows the experimental model (a) and the bonding flow (b). The tin-cap on electrode (T-COTE) was performed by the electroless tin-plating from 0.5μm to 1.0μm in thickness. The argon sputter cleaning was performed before the bonding.

The Si die in 50μm thickness with the copper through-hole electrodes in 20μm pitch was mounted on the interposer as the pre-mount of the first layer. The bonding temperature was 150°C and the bonding force was 24.5N. Then, the Si die with copper bumps in 20μm pitch correspond to the Cu electrodes of the first layer was mounted as the second layer. The bonding temperature was 300°C and the bonding force was 24.5N that were given profile described in Figure 15(b).

Then, the vertical interconnection in 20μm pitch were confirmed at cross-section by SEM. Figure 19 shows the micrographs focused at the interconnection of 1st layer between the copper through-hole electrode and the copper bump on Si interposer. As shown in the figure, the possibilities to realize the micro interconnections utilizing the copper through-hole electrodes in Si devices were confirmed leading to the high-performance 3D stacked LSI in near future.



(a) Experimental Model (b) Bonding Flow

Figure 18 Experimental Model and Bonding Flow of the Vertical Interconnections with Cu TH Electrodes

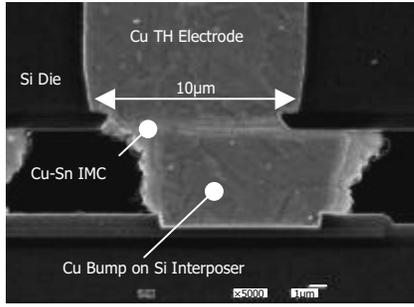


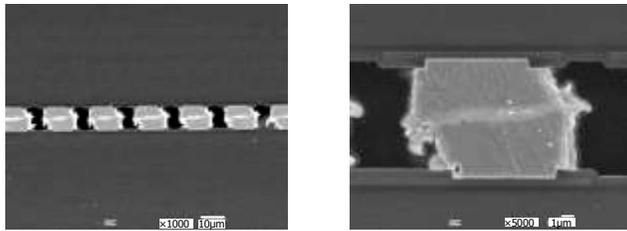
Figure 19 Vertical Interconnection in 20µm pitch

**Feasibilities on Low Temp. Cu Bonding with Tin-plating
-FC Bonding at 150°C in Solid-phase**

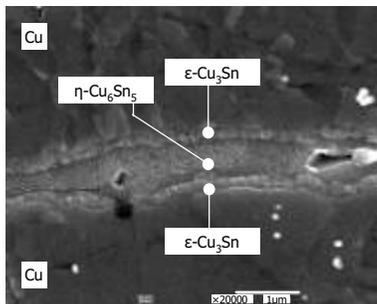
Finally, the feasibility evaluations on the low temperature interconnections utilizing the electroless tin-caps on the copper bumps in 20µm pitch were performed. The same Si dies with the tin-capped copper bumps as shown in Figure 14 were applied to the evaluation. The bonding profile was similar to the temperature and the force as shown in Figure 15(b). The peak temperature at the bonding was set at 150°C to have the micro joining in solid-state and hold down the temperature down to the cure temperature of the underfill resin at 150°C [11] or less, that as a provisional target.

In case that the bonding interface was obtained at 150°C, the IMC layer after the flip-chip bonding was supposed as η-Cu₆Sn₅ from the results so far.

To conform the assumption, first, the bonding interfaces were confirmed at cross sections by SEM. Figure 20 shows the SEM micrographs. Figure 20(a) was focused at the adjacent copper bumps connected in 20µm pitch. Figure 20(b) magnified one of the interconnections between the copper bumps. Figure 20(c) was focused on the IMC layers at the interface between the copper bumps.



(a) Cu Bump Interconnections in 20µm pitch (b) Magnified Cu Bump



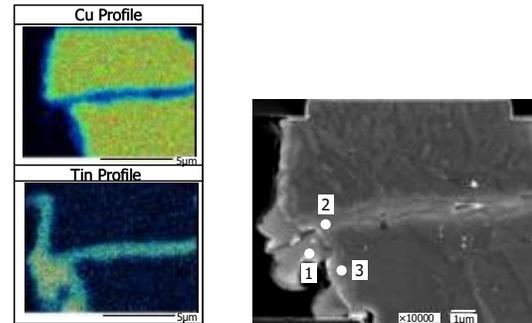
(c) 2-layered IMC between Cu Bumps

Figure 20 SEM Micrographs of Cu Interconnections (150°C)

As shown in the micrographs, it was confirmed that the existence of 2-layered IMC at the interconnections between the copper bumps.

Then, the IMC layer was analyzed by EDS. Figure 21(a) shows the results of EDS mapping for the both profile of tin and copper on the area shown in Figure 21(b). Table 4 shows the results analyzed by EDS on each point from No.1 to No.3 indicated in Figure 21(b) to identify the IMC material from the atomic percentage of the elements. As shown in the results, the IMC layer was confirmed that the 2-layered structures consist of η-Cu₆Sn₅ and ε-Cu₃Sn. Especially, η-Cu₆Sn₅ layer was thicker than that of the interface at 300°C and the IMC layer seemed to be composed of an integrated combination of the symmetry diffusion of the tin from the both layer at the interface.

Finally, the interface at the IMC was analyzed by TEM and ED. The results are indicated in Figure 22. Figure 22(a) shows the image of selected ion monitoring (SIM) after the cutting by the focused ion beam (FIB). Figure 22(b) is a TEM micrograph after thinning and the arrow in the figure describes the magnified point in Figure 22(c), where is the just interface of the bonding layer. Moreover, Figure 22(d) shows the results of ED focused on the circle indicated in Figure 22(c), which is a crystal of IMC at the middle of the bonding layer.



(a) EDS Mapping Data (b) EDS Analysis Points

Figure 21 EDS Analysis at Interconnection (150°C)

Table 4 EDS Analysis at IMC (150°C)

Temp.	試	150		
Point	-	1	2	3
Cu	(at%)	1.4	51.5	50.6
Sn	(at%)	98.6	48.5	49.4
Material	-	Sn	Cu ₆ Sn ₅	Cu ₆ Sn ₅

From the evaluations, it was confirmed the existence of η-Cu₆Sn₅ at the middle of the interface, which suggest the IMC was composed of an integrated combination of the symmetry diffusion of the tin from the both layer in solid-phase. Therefore, the possibilities to have the tin-capped copper bump interconnections at a low temperature in solid phase were proved. Although, the minute voids were found in some portions of the cross-section that were considered as the influence of the oxidation of the tin surface and the uneven

dispersion of the IMC layer [5][10]. The activation and the flattening of the bump surface will be subjects in the future.

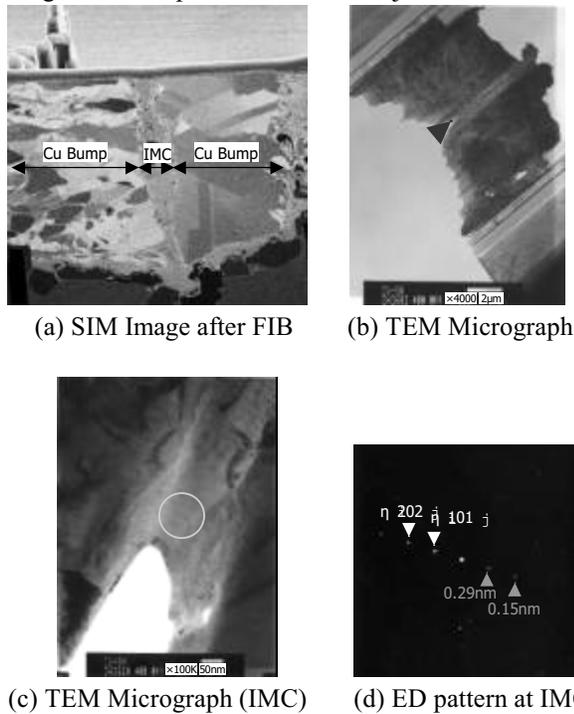


Figure 22 TEM and EDS Analysis at Cu Bump Interconnection (150°C)

-Preliminary Considerations on Low Temp. Interconnection

The IMC layer at 150°C was analyzed by EBSP. Figure 23 shows the result. As shown in the figure, there was no pattern at IMC, which chiefly consist of η -Cu₆Sn₅. It was suggested that there were some remained stress and the defects at this layer. There is fear that the imperfect bonding layer has a bad influence for the micro-joint reliability.

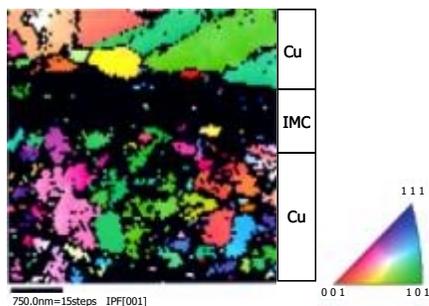


Figure 23 Cross-sectional Analysis by EBSP (150°C)

One of the solutions for the issue, the post-aging process is considered. Figure 24 shows the results of the preliminary evaluation regarding with the effects of the process. Figure 24(a) shows SEM micrograph indicates the bonding layer before aging as incomplete interconnection for the evaluations. The IMC layer was consist of tin and η -Cu₆Sn₅. Figure 24(b) is the cross-sectional SEM micrograph after the aging at high temperature. The variable frequency microwave (VFM) was applied to this evaluation at 300°C in 10 seconds.

As shown in the figure, after the aging, the IMC layer was only consist of ϵ -Cu₃Sn, and in a uniform condition. The aging temperature and the time should be optimized because there were some defects supposable as Kirkendall voids might be caused by rapid diffusion.

However, the consideration of the preferable process to grow the reliable interconnections should be continued also from the standpoint of the productivity in solid-phase diffusion bonding.

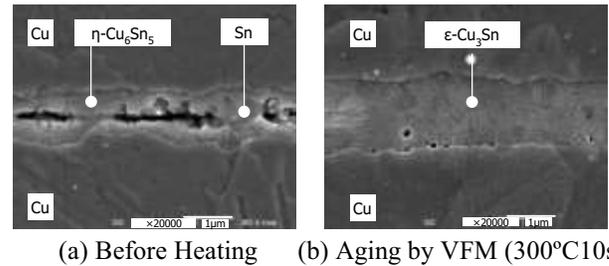


Figure 24 Effect of Post-Aging for the Uniform IMC

Conclusions

- 1) The characteristics of the electroless tin-plating on copper were analyzed by SEM, EPMA, XRD, TEM, ED, EBSP, SERA, and Nano-Indentation. The results are described as in the following;
 - 1-a) The pure-tin layer was easy to disappear due to the diffusion with copper. The diffusion between the η -Cu₆Sn₅ and tin was dominant in the phenomenon, because the η -Cu₆Sn₅ existed as the tin-plating.
 - 1-b) The activation energy was 0.90eV.
 - 1-c) The tin-plating had the crystal orientation at (001) face, even as the copper substrate had no definite orientation.
 - 1-d) The tin-plating could soften the most surface of the bonding interface to control the whole deformation of the bumps leading to the electrical defects. Nevertheless, as the aging time, the roughness of the surface became large.
 - 1-e) From the results, the basic bonding profile was determined to have the lower preheating with the capped copper bumps in 20 μ m pitch.
- 2) The flip-chip bondability with the tin-capped copper bumps in 20 μ m pitch was evaluated. The sufficient interconnection was confirmed. The basic condition was that the bonding temperature at 150°C and the bonding force at 24.5N, in case that the pin-count was 1844pin and the die size was in 10mm square.
- 3) The vertical interconnection between the Cu electrodes through Si die and the adjacent copper bumps on interposer in 20 μ m pitch was evaluated. The possibility to apply the copper bump bonding technologies utilizing electroless tin-caps was confirmed to realize the 3D stacked LSI.
- 4) Feasibilities on the solid-phase diffusion bonding at 150°C were studied with tin-plating on copper. It was

found the integrated combination of the symmetry diffusion of tin from the both layer.

Acknowledgments

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A Fine Pitch COG Technique Using Eutectic Bi-Sn Solder Joints for LCD Driver IC Packaging Applications

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Abstract

We developed the fine pitch COG technique using the eutectic Bi-Sn solder bumps for LCD driver IC packaging. The fine pitch Bi-Sn solder bumps were fabricated using the evaporation method and lift-off process and joined the metal pad on glass substrate. The minimum pitch was 50 μm and the joining temperature was kept below 160°C. The contact resistance of the solder joint of 80 μm pitch was 19 - 35 m Ω , which was much lower than that of the joint made using the conventional ACF bonding technique.

Introduction

Liquid crystal displays (LCD's) are becoming the most important of the display devices, because they combine a compact and flat shape with lower power consumption compared with the traditional cathode ray tubes (CRT's). In the field of LCD's, packaging technology has significant influence on display performance. The electrical interconnect between the LCD and LCD driver circuit needs the improvement to achieve finer pitch, easier assembly, lower joint resistance, and easier reworkability [1]. The chip on glass (COG) techniques are expected to meet these needs and can be used to mount IC's directly on LCD panels[1-3]. The COG technique normally uses the anisotropic conductive films for chip bonding. The COG technique using conventional ACF has a contact resistance on the order of hundred milliohms [4-5]. For high-definition LCD's, contact resistance may be increase because of the decreasing the pixel size and the contact pad size. We developed a new COG technique using the flip chip solder joining technology. The flip chip solder joining technology has the several advantages: fine pitch capability, good electrical performance, and easy reworkability [6]. The commonly used solders such as eutectic Pb-Sn and Pb-5Sn cannot be applied to LCD since the high temperature processing (above 200°C during solder joining) degrades the liquid crystal or the color filter in LCD module. The low temperature solders which can be processed below 160°C should be developed for this application.

We selected the eutectic Bi-Sn (mp : 138°C) solders and developed the COG process using solder joints which can be applicable to LCD. We studied the microstructure of the eutectic Bi-Sn solder bumps and the electrical properties of the solder joints.

Experimental Procedure

Au/Cu/Cr(Ti) thin films were deposited for under bump metallurgy (UBM) using DC magnetron sputtering system on Si wafer. The octagonal UBMs with the pitches of 50 μm and 80 μm shaped were fabricated through the photolithographic process and the wet etching process. For the electrical test of solder joint, new metallization which consists of the UBM and

conductor of the daisy chain is needed. Ti(0.1 μm)/Au(0.1 μm)/Cu(3 μm)/Ti(0.05 μm) metal film was deposited for conductor of the daisy chains on SiO₂/Si wafer. The UBM was fabricated through opening terminal via by wet chemical etching of Ti top layer.

Eutectic Bi-Sn solder bumps were formed on UBM by the evaporation method and the lift-off process using the thick PR solder mask. Fig. 1 shows the overhang-structural solder mask fabricated through two-step spin coating and blank exposure. Reflow process was performed in N₂ using RTA system. The heating rate was 90°C/min and the peak temperature was 160°C. For the glass substrate, the metal pad was formed like UBM process in order to join the chip. For the electrical test, Ti/Au/Cu/Ti or Ti/Au/Ni/Cu/Ti metal films were deposited for conductors of daisy chains on glass substrate. The solder bumped chip was aligned to the metal pads of the glass substrate using a flip chip bonder and all solder joints were made simultaneously during the reflow process. Underfill process was applied to improve the reliability of solder joints. The epoxy resin for underfill required a post cure of 5 minutes at 160°C.

Secondary electron micrographs were observed for the morphology and the microstructure of the solder bumps and joints. The electrical assessment is done using four-point technique to address the electrical resistance of the daisy chain running through the chip and the glass substrate. Fig. 2 is the schematic diagram of the electrical test specimen. One daisy chain has maximum 112 transitions chip/glass substrate.

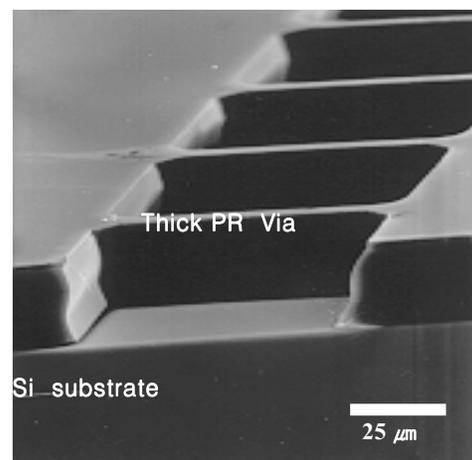


Fig. 1. SEM image of the overhang-structural solder mask.

Results and Discussion

Solder bump formation

Fig. 3 shows the as-deposited solder bumps after removing the solder mask. For the conventional solder mask, the lift-off

was sometimes unsuccessful (Fig. 3-(a)). In the case of overhang structural solder mask, the clean solder bumps were formed (Fig. 3-(b)). The overhang-structural solder mask is the principal factor of the successful lift-off because the overhang structure helps easier strip of the solder mask after solder deposition than the conventional structure.

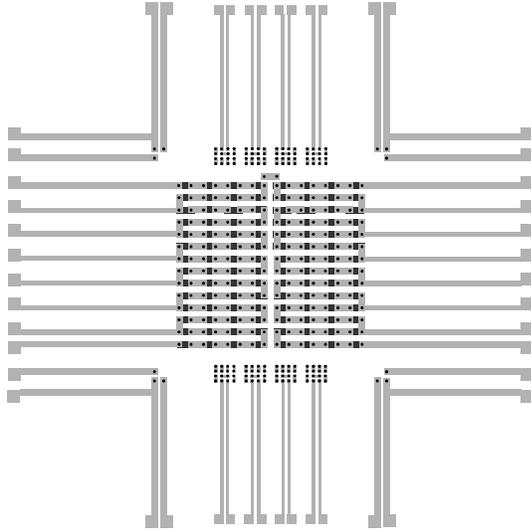


Fig. 2. Placement of daisy chain connection on test chip (dark gray) and substrate (light gray).

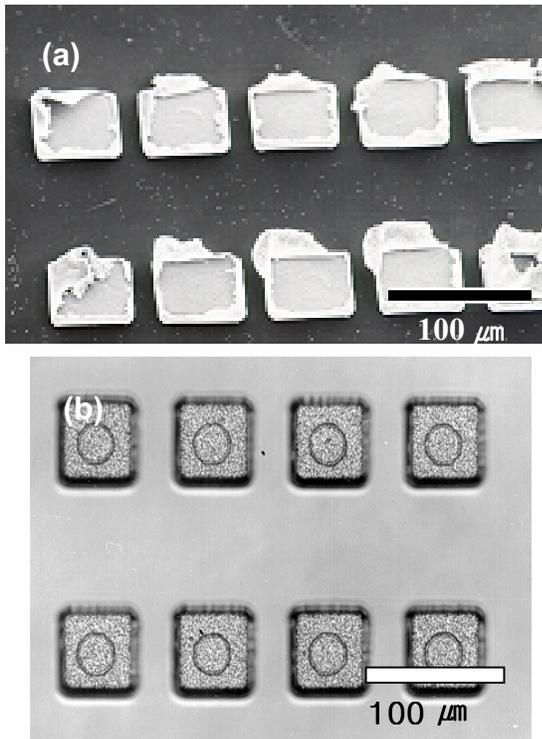


Fig. 3. SEM images of as-deposited solder bumps formed using (a) conventional solder mask and (b) overhang-shaped solder mask.

Fig. 4 is the SEM image showing the eutectic Bi-Sn solder array of the $80\ \mu\text{m}$ pitch after reflow process. The height and diameter of the solder bumps are about $40\ \mu\text{m}$ and $46\ \mu\text{m}$ respectively. Fig. 5 is secondary electron images showing the

Bi-Sn solder bumps reflowed at 150°C and 160°C for 4 min and 9 min. The solders reflowed at 150°C show the rough surface regardless of the reflow time. The solder reflowed at 160°C for 9 min has the smoothest surface. Fig. 6 is the backscattered electron images showing the surface of the eutectic Bi-Sn solder bumps after reflow process. Atomic number contrast can be used to provide more distinguishable microstructure of the eutectic solder because the actual BSE signal increases with the concentration of the heavier element of the eutectic solder. In Fig. 6, the Bi-rich phase appears light and the Sn-rich phase appears dark. The solders reflowed at 150°C consist of the large Bi-rich phases, which were responsible for highly rough surface morphology, on the solder surface. Bi-rich phases are likely to be segregated on the surface of the solder bump because the surface energy of Bi is lower than that of Sn [7]. The solder reflowed at 160°C for 4 min has the mixed surface microstructure which is composed of large Bi phases and lamellar structure. For the solder reflowed at 160°C for 9 min, the microstructure of the surface having smooth morphology appears lamellar structure similar to that of the eutectic Pb-Sn. When the mixtures of Bi and Sn directly evaporate, the as-deposited Bi-Sn solder bump has the layer structure because Bi having low vapor pressure is deposited earlier than Sn having high vapor pressure. During the reflow process, the two phases are mixed with each other. As the reflow time gets longer, Bi and Sn can be easily mixed and solder bumps have more smooth surface and finer lamellar structure because the volume of the liquid phase increases during the reflow process.

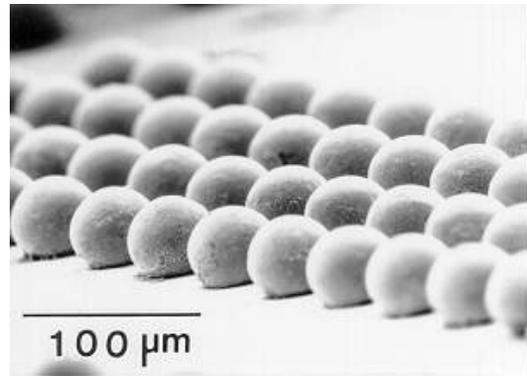


Fig. 4. SEM images of $80\ \mu\text{m}$ pitch Bi-Sn solder bump array.

Fig. 7 is the backscattered electron images showing the cross-section of Bi-Sn solder bumps. Only the solder reflowed at 160°C for 9 min appears the clear lamellar structure and the others consist of large Bi-rich phases in a Sn matrix. The surface of the solder bump is mainly composed of the segregations of Bi-rich phases like Fig. 6-(a), (b) and the interior has relatively uniform mixture of two phases. In Fig. 7-(a) and (c), faceted Bi particles like fine plate are observed in a Sn matrix. Bismuth is one of the typical materials having high entropies and can be faceted [8]. The fine plate-like precipitates are caused by the decrease in solid solubility of Bi in Sn as the solder is cooled. In phase diagram of Bi-Sn alloy,

the solubility of Bi in Sn reduces sharply from 21wt% at the eutectic melting point to about 4 wt% at 20 °C.

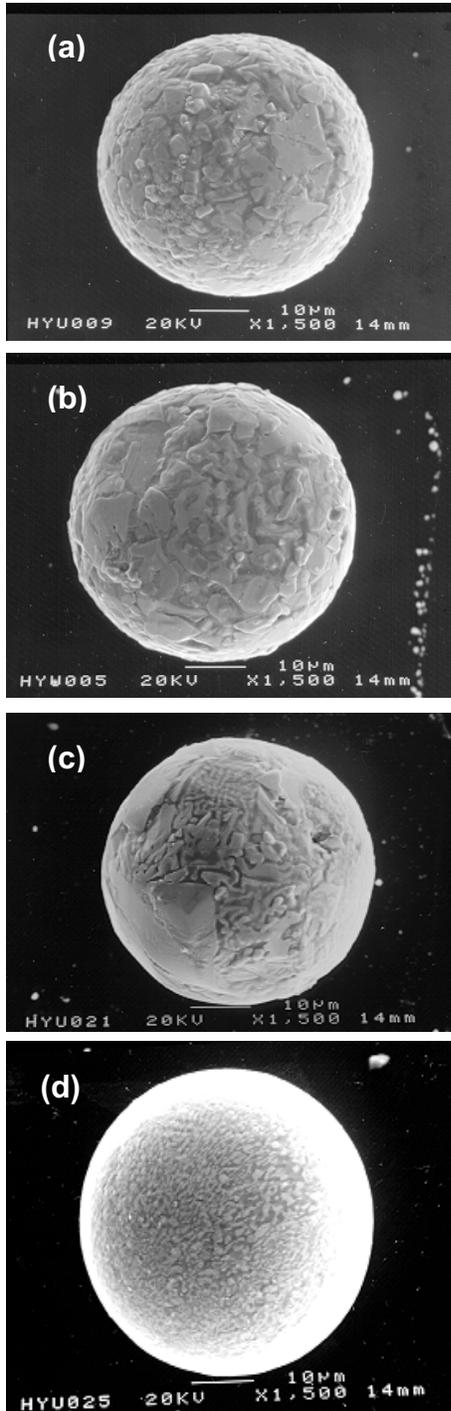


Fig. 5. SEM micrographs showing the plane view of the Bi-Sn solder bumps after reflow (a) at 150 °C for 4 min, (b) at 150 °C for 9 min, (c) at 160 °C for 4 min, and (d) at 160 °C for 9 min.

In general, the solder microstructure depends on the cooling rate from the melt as well as the reflow time. The effect of the cooling rate on the microstructure of the Bi-Sn solder bumps was investigated. The reflow profiles with different cooling rates were shown in Fig. 8. Fig. 9 is the SEM micrographs showing the Bi-Sn solder bumps reflowed at

160 °C for 4 min with cooling rate. The solder bump reflowed at slow cooling rate shows the rough surface and the solder bump reflowed at rapid cooling rate has the smoothest surface. Fig. 10 is the backscattered electron images showing the cross-section of Bi-Sn solder bumps reflowed at 160 °C for 4 min with cooling rate. All solder bumps consist of the mixture of two phases and the large Bi phase. As the cooling rate gets faster, the solder bump has more uniform mixture of two phases and smaller Bi phase.

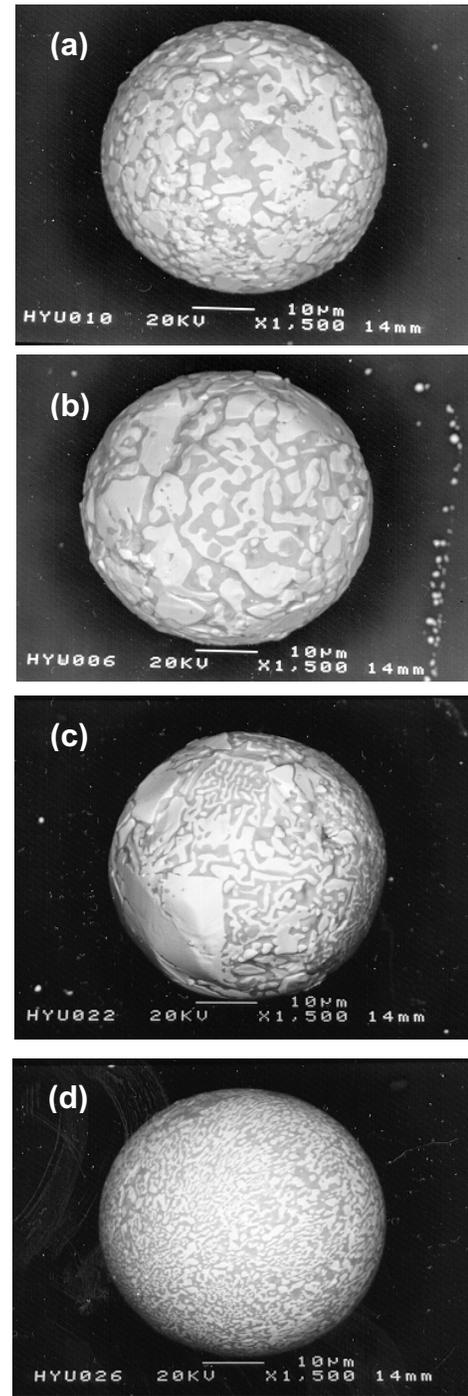


Fig. 6. Backscattered electron images of the Bi-Sn solder bumps after reflow (a) at 150 °C for 4 min, (b) at 150 °C for 9 min, (c) at 160 °C for 4 min, and (d) at 160 °C for 9 min.

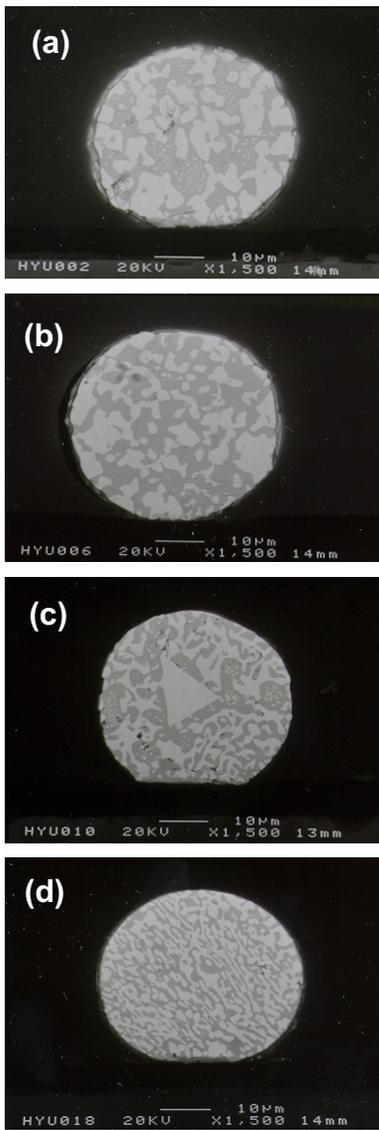


Fig. 7. Backscattered electron images showing the cross-section of the Bi-Sn solder bumps after reflow (a) at 150 °C for 4 min, (b) at 150 °C for 9 min, (c) at 160 °C for 4 min, and (d) at 160 °C for 9 min.

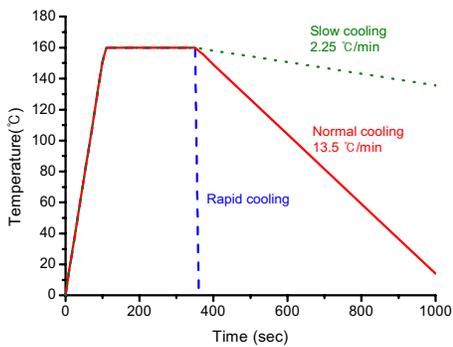


Fig. 8. Reflow profiles of the Bi-Sn solder bumps with different cooling rates.

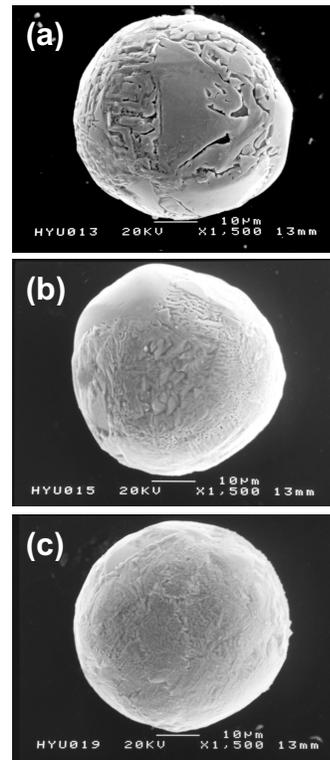


Fig. 9. SEM micrographs showing the plane view of the Bi-Sn solder bumps after reflow (a) at slow cooling rate, (b) at normal cooling rate, and (c) at rapid cooling rate.

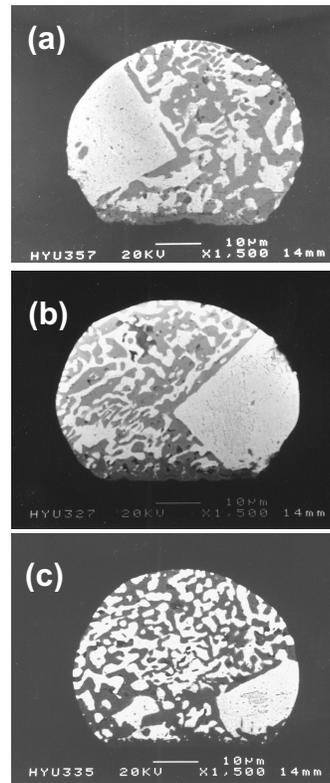


Fig. 10. Backscattered electron images showing the cross-section of the Bi-Sn solder bumps after reflow (a) at slow cooling rate, (b) at normal cooling rate, and (c) at rapid cooling rate.

The test chips were mounted on the glass substrates using the joining reflow at 160°C. Fig. 11 is the SEM micrograph showing the 80 μm pitch Bi-Sn solder joint assembled at 160°C. Fig. 12 is one example of the 50 μm pitch solder joints assembled at 160°C. The spherical-shaped solder joint is connected through the metallization between Si and glass substrate.

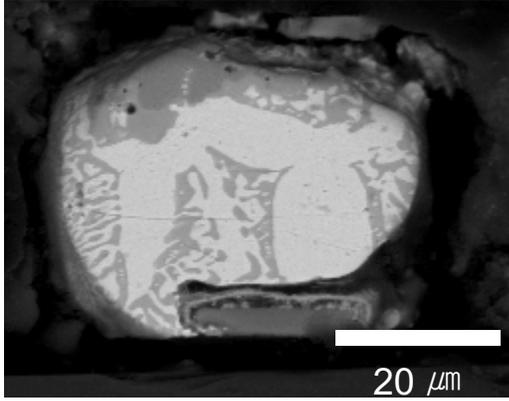


Fig. 11. Backscattered electron image showing the Bi-Sn solder joint of 80 μm pitch.

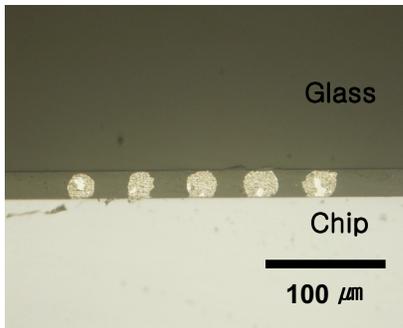


Fig. 12. Optical image showing the solder joints of 50 μm pitch.

Table 1 shows the average contact resistances (R_c s) of Bi-Sn solder joints with Au/Cu/Ti and Au/Ni/Cu/Ti metal pads of the glass substrate. The R_c was measured using Bi-Sn solder joints having a minimum 80 μm pitch. The average R_c s were obtained from at least 3 specimens. As can be seen from Table 1, the R_c s of Bi-Sn solder joints with Au/Cu/Ti and Au/Ni/Cu/Ti metal pads of the glass substrate are 18.6 mΩ and 34.6 mΩ, respectively. These values include the contact resistance of the solder joints and the resistance of the conductor trace on chip and substrate. These values are much lower than the contact resistance in the conventional ACF bonding which is the order of hundred milliohms. If the resistances of the conductor trace on chip and substrate is calculated and removed from the R_c s presented in Table 1, the real contact resistances of Bi-Sn solder joints with Au/Cu/Ti and Au/Ni/Cu/Ti metal pads are 8.1 mΩ and 12.0 mΩ, respectively. This indicates that the resistance of Au/Ni/Cu/Ti metallization is larger than that of Au/Cu/Ti metallization and the real contact resistances of the Bi-Sn solder joints are almost same in both specimens.

Table 2 shows the R_c s of Bi-Sn solder joint before and after underfill process. The epoxy resin for underfill required a post cure of 5 minutes at 160°C. After the underfill process, the R_c of Bi-Sn solder joint slightly increased but it remained within the range of standard deviation. This value is also much lower than the contact resistance of conventional ACF bonding.

Table 1. Contact resistance of Bi-Sn solder joint before underfill process.

Glass metallization	R_c (mΩ)	Standard deviation
Au/Cu/Ti	18.6	3.0
Au/Ni/Cu/Ti	34.6	6.3

Table 2. Contact resistance of Bi-Sn solder joint before and after underfill process.

Glass metallization	Underfill	R_c (mΩ)	Standard deviation
Au/Cu/Ti	X	19.5	4.1
	O	23.4	6.7

The R_c s of the Bi-Sn solder joint without and with underfill process were measured after storage at a hot humidity (85°C/85% RH) environment. The results are shown in Table 3. The R_c of the Bi-Sn solder without underfill increased twice as large as the initial value after 500 hrs. On the other hand, The R_c of the Bi-Sn solder joint with underfill is almost the same even after 500 hrs. In Table 3, it is found that the underfill process improves the reliability of the solder joint.

Table 3. Contact resistance of Bi-Sn solder joint without and with underfill after storage at 85°C/85% RH condition.

Glass Metallization	Under-fill	Storage time	R_c (mΩ)	STD
Au/Cu/Ti	X	0 hr	19.4	2.4
		100 hr	23.0	1.2
		250 hr	37.6	2.7
		500 hr	39.3	4.4
	O	0 hr	15.5	1.1
		100 hr	15.9	0.8
		250 hr	16.3	0.6
		500 hr	17.3	1.8

Conclusions

Using eutectic Bi-Sn solder materials, we developed the COG technique of 50 - 80 μm pitch at the temperature below 160°C. The overhang-structural solder mask is effective for perfect lift-off. As the reflow time gets longer and the cooling rate gets faster, the solder bumps have more smooth surface and more uniform mixture of Bi and Sn. The contact resistance of Bi-Sn solder joint having a minimum 80 μm pitch was 19 -35 m Ω . The R_c of the Bi-Sn solder joint with underfill did not change even after hot humidity test.

The COG technique using the low temperature solder bumps has the several advantages compared with the COG technique using the ACF:

- 1) It is easy to be used in ultra-fine pitch applications due to the self-alignment of liquid solder.
- 2) The solder bumps form metallurgical junctions between metal substrates, whereas the ACFs forms mechanical bonds at the substrate surface.
- 3) The bonding pressure of solder bumped flip chip bonding is lower than that of ACF bonding. An excessive pressure on bumps can cause glass breakage.
- 4) The rework process is easy by raising the temperature above the melting temperature of solder.
- 5) It can lower the material cost because ACF does not need.

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Pb-Free Bumping Technology and UBM (Under Bump Metallurgy)

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Abstract

Today, the demand of Pb-free and high density interconnection technology is rapidly growing. The electroplating bumping method is a good approach to meet fine pitch requirements especially for high volume production. This paper suggests a Sn/3.5Ag Pb-free electroplated bumping process for the high density Pb-free interconnection. The Sn/3.5Ag alloy electroplating process was successfully developed in the cooperation between KAIST and Fraunhofer IZM.

Another important issue for the future flip chip interconnection is to optimize UBM (Under Bump Metallurgy) system for high-density and Pb-free solder bumps. In this work, 4 different types of UBM systems, sputtered TiW 0.2 μ m/Cu 0.3 μ m/electroplated Cu 5 μ m, sputtered Cr 0.15 μ m/Cr-Cu 0.3 μ m/Cu 0.8 μ m, sputtered NiV 0.2 μ m/ Cu 0.8 μ m, sputtered TiW 0.2 μ m/ NiV 0.8 μ m, were selected, processed, and compared the interfacial reaction of electroplated Pb/63Sn and Sn/3.5Ag solder bumps. Both Cu-Sn or Ni-Sn IMC (Intermetallic Compound) growth showed a tendency to spall-off from the UBM/Solder interface when the solder wettable layer was all consumed during liquid state 'reflow' process. This IMC spalling mechanism appeared different depending on the barrier layer material.

Introduction

• Bumping Technology

When the flip chip interconnection method was first introduced by IBM in early 1960, the evaporation method was adopted for solder bump deposition. But this method is known as a very high cost process and has a limitation to process on large size wafer due to thermal mismatch problem [1]. In today's wafer level solder bumping, there are two main process categories: solder paste stencil printing and electroplating methods. The stencil printing method is a good approach for large pitch (> 150 μ m) and low cost bumping. Easy to adopt new solder material is another main advantage of the stencil printing process. The electroplating method is

considered relatively expensive due to its lithography process but it is a good solution for fine pitch, small bump size, high yield, high volume production, and large wafer size [2]. The demand for high density and fine pitch interconnection technology is continuously growing. This plating method is accepted by companies for high volume production and the market is growing as well. But the solder material and UBM change is not easy to compare to the stencil printing method. Therefore, this study is mainly focused on the bumping process and UBM development for electroplating method.

• Solder Material

The currently used lead-containing solders are a potential risk to the global environment and the use of Pb in electronics will be prohibited by law in Japan in 2005 and in Europe in 2008 according to the WEEE (Waste from Electronic and Electrical Equipment) 3rd proposal [3]. Nowadays, Sn/Ag/Cu solder is considered as a major candidate of Pb-free solder material. However, electroplating of three component system has not been fully realized in today's technology. In this study, Sn/3.5Ag solder was selected as an alternative to replace the eutectic Pb/63Sn for electroplated bumping material. Many studies have been reporting the advantages and disadvantages of each Pb-free solder material. Comparing with Sn/0.7Cu, the Sn/3.5Ag has an advantage for better wettability, and this is a very important issue because the wetting problem can be a serious problem especially for small size bump assembly. Besides, Sn/3.5Ag has slightly lower melting temperature (221 °C) than Sn/0.7Cu system (227 °C).

• UBM (Under Bump Metallurgy)

For flip chip bumping technology, especially in the case of electroplated bumps, the selection of a proper UBM is very important because it serves not only the typical purpose of UBM such as solder adhesion layer, diffusion barrier, adhesion promoter but also has to meet technological requirements like serving as plating base which should be etched after plating in the presence of solder bumps.

To select a proper UBM system for electroplated solder bumping process, the following issues should be addressed:

- The stress of UBM should be optimized to avoid film delamination, chip/UBM failure, or Si cratering.
- The selective etching condition of UBM must be provided in the presence of plated or reflowed solder bumps
- The full understanding of UBM/solder interface IMC growth behavior during process and usage is needed especially for Pb-free and fine-pitch interconnection.
- The UBM structure should serve as an effective diffusion barrier between chip pad and solder bump.
- The electrical contact resistance of UBM/solder should be minimized.
- The metallurgy and the deposition method should be as simple as possible for the process cost down.

Among the above mentioned issues, the UBM film stress, UBM/solder interface IMC growth behavior, diffusion barrier characteristics will be discussed in this paper.

II. Experimental

II-1. Bumping Process

The four UBM systems were selected as shown in Table I. The each UBM metallurgy was deposited sequentially using Batch Sputter System LLS EVO (Unaxis) without breaking the vacuum. Four 6 inch dummy oxide and four 6 inch test pattern wafers were prepared for each UBM and half of them were electroplated with Sn/3.5Ag and the other two with Pb/63Sn. The mask pattern for the lithography process has octagonal openings with sizes of 80 μm and 130 μm and with a pitch of 100 ~ 300 μm . Photoresist with a thickness of 30~60 μm has been patterned using AZ4562. The height of plated bumps was controlled in the range of +/- 5 μm of the PR thickness. After the Sn/3.5Ag or Pb/63Sn plating process, the photoresist was removed and the layers used as plating base were selectively etched. The undercuts beneath the bumps were controlled less than 2 μm on both center and periphery bumps of the wafers. The detailed electroplating process of eutectic Pb/63Sn bumps is described in our previous publications [6, 7].

Table I. Selected UBM Systems for the Study

UBM	Thickness (μm)
TiW / Cu / electroplated Cu	0.2/ 0.3/ 5
Cr / Cr-Cu / Cu	0.15/ 0.3/ 0.8
NiV / Cu	0.2 / 0.8
TiW / NiV	0.2 / 0.8

The newly developed Sn/3.5Ag alloy electroplating condition for bumping was used [8]. According to our investigation, the plated SnAg composition was quite different on the wafers with and without printed photoresist pattern. The Ag composition in bump is decreasing with increasing current density, which is typical behavior of codeposition mechanism, as indicated in Fig.1. Fig.2 shows the deposited Sn/3.5Ag bump before and after the reflow process at 250 $^{\circ}\text{C}$.

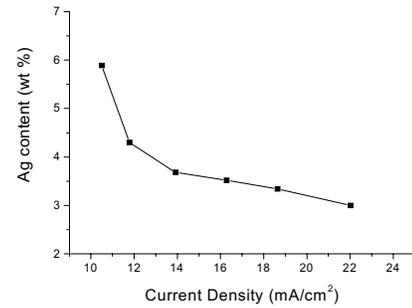
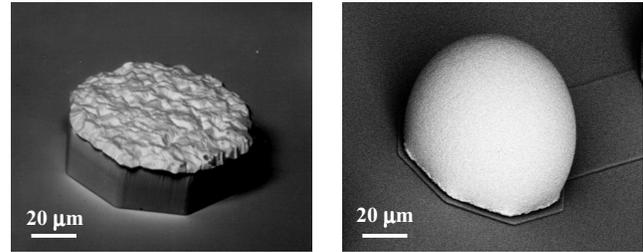


Fig. 1 Effect of current density on the Ag content for bump plating



(a) plated Sn/3.5Ag bump

(b) Sn/3.5Ag bump after reflow

Fig. 2 SEM images of alloy plated Sn/3.5Ag solder bumps

II-2. Sample Preparation for Interface Analysis

Before starting the sample preparation for interface reaction study, EDX analysis was carried out for each wafer to check their composition. The compositions were detected in the range of (3.5 +/-1) wt.% Ag for Sn/3.5Ag and (63 +/-6) wt.% Sn content for Pb/63Sn. 20 dummy chips from the center part and other 20 chips from periphery of each 6 inch wafer were chosen for each wafers. The samples were reflowed in organic medium at (210 +/-5) $^{\circ}\text{C}$ for Pb/63Sn and at (250 +/-5) $^{\circ}\text{C}$ for Sn/3.5Ag for 1, 5, 10, and 20 min to study the relation between interfacial reaction. The convection oven is used for solid state aging treatment. The cross-sectional samples were prepared with 100 μm size bumps. The Scanning Electron Microscopy (SEM) and the Energy Dispersive X-ray (EDX) were used to examine the cross-sectional micro-structural morphology and composition of IMC layer at the interface between UBMs and solder. The AES (Auger Electron Spectroscopy) depth profile was applied to investigate the diffusion behavior of stacked UBM layers.

III. Results and Discussions

III-1. UBM Stress

The residual stresses in UBM system should be considered more important technical issue with increasing wafer size trend today. Excessive tensile stresses can produce film and substrate cracking, whereas compressive stress can produce film decohesion by buckling [9]. Generally, the films deposited by sputtering show a tendency to have compressive stress caused by "atomic peening effect", the bombardment of the film surface by energetic species, compared to the films by evaporation [10]. In the UBM study for bumping, *Datta et al.* reported the sputtered Cr/CrCu/Cu UBM, with slightly compressive stress, is preferred for electroplated Pb/95Sn solder bumps than

evaporated layers because of the stronger adhesion behavior [11].

In the beginning of this work, we found the peel-off problem of as sputter deposited film for TiW 2000 Å/ NiV 8000 Å on patterned wafer. The dummy wafers deposited in the same condition didn't show any peel-off problem. Korhonen also reported that they were able to deposit only about 5000 Å of Ni via evaporation on top of Cr without causing peeling off of the Ni layer [12]. Of course, the film stress can be controlled by deposition parameters such as gas pressure and bias voltage, and the deposition condition for TiW 2000 Å/NiV 8000 Å was finally optimized for this study. After the parameter optimization, the stresses of 4 UBM systems were measured by Dektak Stylus Profiler using bending plate method and Stoney equation [13, 14]. For each UBM combination, 4 dummy and 4 patterned 6 inch wafers were measured and the values are summarized in Fig. 3. The first TiW/Cu UBM indicates only sputtered layers without Cu plating and shows compressive stress. However, the other three UBMs show tensile stresses. As we expected, the TiW 2000 Å/NiV 8000 Å shows the highest tensile stress even after the process optimization.

Generally, the total residual stress in a film consists of the intrinsic stress, caused by film structure and the presence of impurities, and the thermal stress by CTE (Coefficient of Thermal Expansion, α) mismatch between film and substrate.

$$\sigma_{\text{thermal}} = E_f (\alpha_s - \alpha_f) \Delta T / (1 - \nu_f) \quad (1)$$

where E_f is the Young's modulus of the film, α_s and α_f are CTE of the substrate and the film, and ν_f is the Poisson's ratio of the film. Comparing the α and E_f of Cu and Ni¹, it can be seen that the high stress of Ni is not caused by thermal stress because Cu has even higher values. Therefore, the high stress of Ni film is mainly intrinsic stress. *Klokholm* revealed the metal films with higher melting point and higher shear modulus such as Ni, V, Fe, Co, Mn showed higher internal stress than Ti, Cu, Au, and Ag in case of evaporation [15]. It is strongly believed that the Ni thin film has a tendency to have high intrinsic tensile stress because of its deposition growth behavior such as columnar structure growth. And the use of thick Ni UBM layer should be carefully controlled.

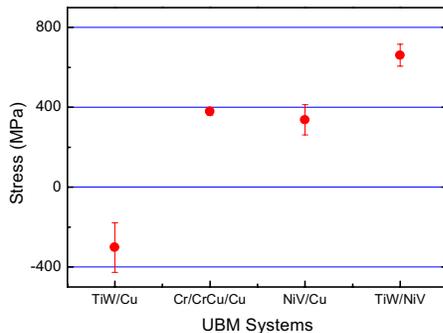


Fig. 3 Measured Stress of each UBM systems after the stress optimization for TiW/NiV UBM Measured using 6 inch wafers

¹ CTE of Cu : 16.5 x 10⁶/K, Ni: 13.4 x 10⁶/K, Young's Modulus: Cu:300, Ni:213

III-2. Interface Intermetallic Growth Behavior

A. TiW/Cu/ep.Cu UBM

The TiW/Cu/electroplated Cu UBM is one of the most commonly used metallurgy structure for electroplated bumping process. TiW (10Ti-90wt%W) layer is known to have better diffusion barrier property than Ti or Cr. Normally, more than 5 μm thick Cu is needed to avoid total Cu consumption which may cause the solder bump detachment by IMC growth during the process or usage. The reported disadvantages of this UBM are: First, the thick Cu-Sn IMC layer can cause stress induced crack site between soft solder and hard IMC. Secondly, the Si cratering. However, this UBM is still one of the most commonly used UBM especially for electroplating bumping process because its process is well established and is suitable to other plated bumping material. Numerous studies have been reported on Cu and Sn containing solder interface. Double layered Cu₆Sn₅ and Cu₃Sn IMC phases can be seen at the interface in normal 'liquid state solder reflow' or 'solid state aging' condition. Generally, the Cu₆Sn₅ IMC is the first forming phase between Cu and solder because it has highest driving force [16] and lower activation energy than Cu₃Sn in normal reflow temperature range [17-19]. The shape of Cu₆Sn₅ IMC appears so-called scallop-like grains in the liquid solder reflow condition. The Cu₃Sn IMC is formed between Cu and Cu₆Sn₅ if the Cu supply is not limited [20].

In this study, we compared the IMC growth behavior with 100 μm size electroplated Pb/63Sn and Sn/3.5Ag solder bumps. Fig. 4 shows the cross-sectional images of Pb/63Sn and Sn/3.5Ag in different heat treatment condition. The consumed Cu thickness and the average Cu-Sn IMC thickness are summarized in Table II and III, respectively. Likewise other studies, the Sn/3.5Ag solder shows higher Cu-Sn IMC growth rate than Pb/63Sn solder because of higher Sn content and higher reflow temperature. The effect of high Sn content solder material on IMC growth rate was found to be bigger than high temperature effect; Through the same temperature reflow test at 250 °C for both Pb/Sn and Sn/Ag, we have found that Sn/3.5Ag solder still showed thicker IMC layer than Pb/63Sn. In the IMC morphology, the Cu-Sn IMC crack has been found when the IMC thickness is over 2 μm . The Cu-Sn IMC has been known as very hard material (Vickers hardness: 378 +/- 55, Young's Modulus: 85.56 +/- 1.65 [21]). So, the excessive stress formation during IMC growth can be expected and presumably causes the IMC cracks.

One interesting fact should be noted in this UBM study. The consumed Cu thickness of 20 min reflow and 1000 hours aging are similar as shown in Table II; 2.20 μm and 2.29 μm for Pb/63Sn solder, 3.73 μm and 3.80 μm for Sn/3.5Ag. But the average Cu-Sn IMC thickness of those are quite different in Table III; 2.10 μm and 3.68 μm for Pb/63Sn, and 4.78 μm and 5.27 μm for Sn/3.5Ag. This behavior can also be noticed when we compared the IMC thickness in Fig.4(c) and in Fig.4 (e) for Pb/63Sn; in Fig.4 (d) and in Fig. 4 (f) for Sn/3.5Ag. The Cu dissolution in the liquid state reflow is very fast.

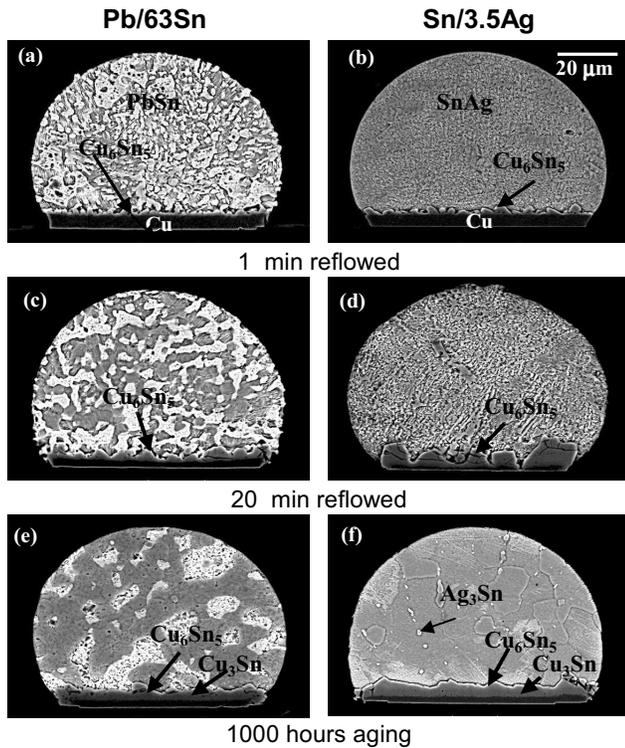


Fig.4 Cross-sectional SEM images of eutectic PbSn and SnAg solder bumps on TiW/Cu/ep/Cu UBM (a) PbSn after 1 min reflow at 210 °C (b) SnAg after 1 min reflow at 250 °C (c) PbSn after 20 min reflow at 210 °C (d) SnAg after 20 min at 250 °C (e) PbSn after 1 min reflow at 210 °C followed by 1000 hours annealing at 125 °C (f) SnAg after 1 min reflow at 250 °C followed by 1000 hours annealing at 150 °C

Table. II Consumed Cu thickness (μm)

	1 min reflow	20 min reflow	1 min reflow + 1000 hr aging
Pb / 63Sn	0.69 +/- 0.17	2.20 +/- 0.33	2.29 +/- 0.32
Sn /3.5Ag	1.20 +/- 0.16	3.73 +/- 0.36	3.80 +/- 0.36

Table. III Average IMC thickness (μm)

	1 min reflow	20 min reflow	1 min reflow + 1000 hr aging
Pb / 63Sn	0.93 +/- 0.16	2.10 +/- 0.26	3.68 +/- 0.33
Sn / 3.5Ag	2.30 +/- 0.38	4.78 +/- 0.66	5.27 +/- 0.49

The channel between IMC grains, indicated in Fig.5, is believed as the main Cu diffusion path to solder and vice versa. In solid state high temperature aging condition, the IMC grows as a layered structure and the channels are disappearing as shown in Fig.4 (e) and (f). Therefore, the diffused Cu atoms from the plated Cu can not easily diffuse to the solder because the layered Cu-Sn IMC can act as a diffusion barrier. But in liquid state solder condition, during reflow, the IMC has the thin channel sites. So, the Cu atoms can diffuse more easily to the solder side. Another factor to be considered is that the diffusivity of Cu in liquid solder (normally in the range of 10^{-5} cm²/s) is much faster than in solid solder (in the range of 10^{-9} cm²/s) [22]. Therefore, the Cu diffusion deep into the top side solder is much favorable in liquid solder state. The EDX analysis of solder top area of 20 min reflowed samples were higher than that of 1000 hours

aged samples. (2.604 +/- 0.907 wt.% Cu for 20 min reflowed and 1.448 +/- 0.234 wt.% Cu for 1000 hr aged). Choi also reported that the Cu diffusion into 100 micron from the Cu/solder interface with multiple reflow times and detected over 3 at. % Cu after four times reflow at 250 °C with Sn/3.5Ag [23].

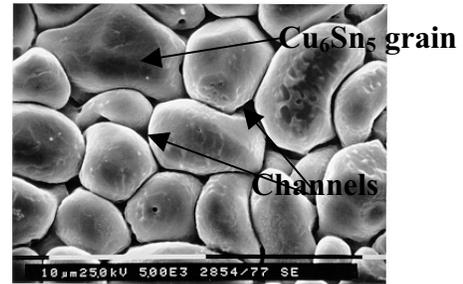


Fig. 5 Top-view SEM micrographs of grain morphology of Cu-Sn IMC of 63Sn-37Pb on TiW/Cu/ep.Cu UBM reflowed at 210 °C for 10 min

B. Cr/CrCu/Cu UBM

When the flip chip interconnection method, C4 (Controlled collapse chip connections), was first introduced by IBM, the thin-film multiplayer Cr/Cu/Au UBM was used for high Pb content solder. The Cr was used as an adhesion layer, the Cu was adopted as solderable layer, and the final Au flash was used to inhibit surface oxidation. However, the following studies revealed that the solder has a tendency to dewet from the Cr surface when the Cu layer is totally consumed by Cu-Sn IMC growth [24,25]. Therefore, the phased CrCu layer by evaporation was introduced between Cu and Cr layers and was expected to serve as an adhesion enhancement layer by lock-in effect [26]. This UBM has been reported to have good interface stability with high Pb content solders – Pb/5Sn and Pb/3.5Sn –, but recent studies reported that the phased CrCu layer with Pb/63Sn solder also showed the Cu-Sn IMC spalling after long time reflow and it may cause dewetting of solder [27,28].

In this study, the Cu-Sn IMC growth behavior was compared using Pb/63Sn solder and Sn/3.5Ag solder with increasing reflow time and solid state aging time. In Fig.6(a), (c), the Cu-Sn IMC was formed at the solder/UBM interface after 1 min reflow, but the big and few Cu-Sn IMC grains were about to spall from the interface after 20 min reflow at 210 °C with Pb/63Sn solder. In case with Sn/3.5Ag solder, the Cu-Sn IMC spalling was already appeared just after 1 min reflow at 250 °C as shown in Fig.6 (b). After 20 min reflow with Sn/3.5Ag in Fig.6 (d), the big Cu₆Sn₅ IMC phases could be detected inside the solder bump not at the interface. The Cu-Sn IMC is heavier than solder; the density of Cu₆Sn₅ IMC was reported as about 8.28 +/- 0.02 g/cm³ [29] and the calculated density of Sn/3.5Ag solder is 7.081 g/cm³ at 250 °C reflow temperature [30,22]. Therefore, the driving force to lift the spalled Cu-Sn IMC is not the density difference or gravity but presumably due to the liquid solder fluidity.

The remaining UBM layer after IMC spalling has very little Cu content through the AES depth analysis, this means the Cu in the Cr-Cu compound layer was also consumed by IMC growth.

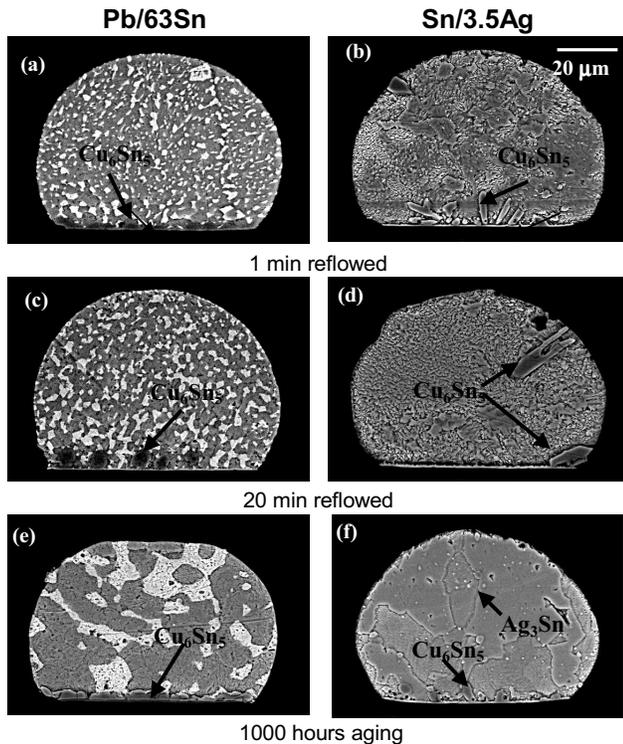


Fig.6 Cross-sectional SEM images of eutectic PbSn and SnAg solder bumps on Cr/CrCu/Cu UBM (a) PbSn after 1 min reflow at 210 °C (b) SnAg after 1 min reflow at 250 °C (c) PbSn after 20 min reflow at 210 °C (d) SnAg after 20 min at 250 °C (e) PbSn after 1 min reflow at 210 °C followed by 1000 hours annealing at 125 °C (f) SnAg after 1 min reflow at 250 °C followed by 1000 hours annealing at 150 °C

The solid state aging test for 1000 hours at 125 °C with Pb/63Sn solder in Fig. 6 (e) does not show the Cu-Sn IMC spalling from the interface. The Cu-Sn IMC morphology after 1 min reflow in Fig.6 (a) does not develop to the scalloped shape with channels but the channels were disappeared and grows as a layered structure with increasing aging time, which already mentioned in TiW/Cu/ep.Cu UBM case. The spalled IMC morphology of aged Sn/3.5Ag bump is still similar to that of 1 min reflow and stayed near the interface as shown in Fig.6 (f). This means the Cu-Sn IMC grains does not have enough freedom to change their surface morphology in solid state solder surrounding, this can be correlated to the layer shaped IMC growth rather than channel development nor spalling in solder state aging.

C. NiV/Cu UBM

The Al/NiV/Cu UBM system was introduced by Delco Electronics and is used for screen printed solder bumps [31]. The 7 ~ 8 wt.% V is added to Ni in order to increase the magnetron sputtering yield because the pure Ni is ferromagnetic material. The basic idea of Ni containing metallurgy in UBM structure is that the Ni forms IMC with Sn but the IMC growth rate is slower than the most commonly used metallurgy Cu. In this UBM, Al was used as an adhesion layer to Al pad and passivation layer (oxide, BCB, or polyimide material), NiV is introduced as a buffer layer to inhibit Cu-Sn IMC spalling and dewetting issue, and the final Cu is used as solderable surface. *Liu et al.* reported

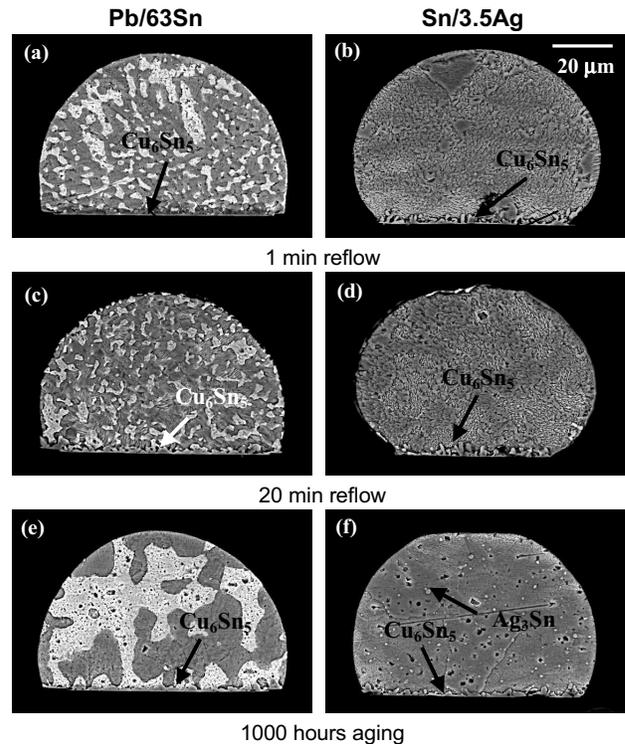


Fig.7 Cross-sectional SEM images of eutectic PbSn and SnAg solder bumps on NiV/Cu UBM (a) PbSn after 1 min reflow at 210 °C (b) SnAg after 1 min reflow at 250 °C (c) PbSn after 20 min reflow at 210 °C (d) SnAg after 20 min at 250 °C (e) PbSn after 1 min reflow at 210 °C followed by 1000 hours annealing at 125 °C (f) SnAg after 1 min reflow at 250 °C followed by 1000 hours annealing at 150 °C

stable adhesion between Cu_6Sn_5 IMC and Ni(V) using screen printed Pb/63Sn solder bump [32], and the similar Al/Ni/Cu UBM structure showed good interface stability in our previous UBM investigations using plated eutectic PbSn [7] and eutectic SnBi bumps as well [33].

We adopted this NiV/Cu UBM to the electroplated Pb/63Sn and Sn/3.5Ag material without Al layer in case of test wafers because the selective etching of Al in the presence of Sn-rich solder was not optimized yet. But the test chip already had Al metallurgy and we couldn't find any delamination or Al/NiV interface failure by the bump shear test after the whole process. In our investigation, there was no Cu-Sn IMC spalling even after 20 min reflow with high Sn content Sn/3.5Ag solder as shown in Fig.7 (d). However, if we increase the reflow time over 20 min, many Sn/3.5Ag solder bumps were lost and the remaining layer was detected as Al layer. It should be noted that *Liu et al.* reported small reaction of NiV with Sn through their TEM investigation on Al/NiV/Cu UBM with Pb/63Sn solder after 10 min reflow at 200 °C [32]. Therefore, further reaction of NiV, underneath the Cu, with Sn can be expected, when higher Sn-content Sn/3.5Ag and higher reflow temperature are used. However, the Cu-Sn or Cu-Ni-Sn IMC spalling phenomena was not exactly detected among the 1, 10, 20, 30, 40, and 60 min reflowed samples. Over 20 min reflowed samples have few remained bumps and are believed the total consumption of Cu and Ni causes to the dewetting of solder immediately.

This is quite different from the IMC spalling behavior of Cr/Cr-Cu/Cu UBM and the following TiW/NiVUBM.

D. TiW/NiV UBM

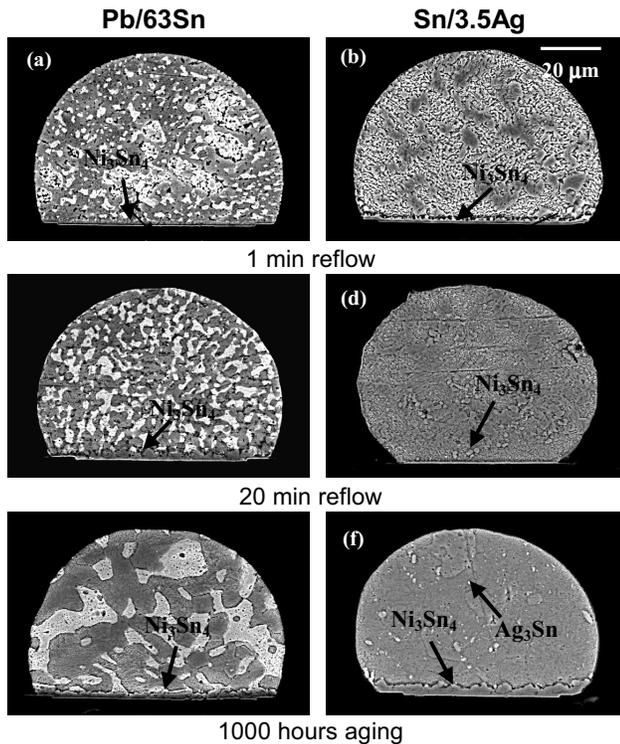


Fig.8 Cross-sectional SEM images of eutectic PbSn and SnAg solder bumps on TiW/NiV UBM (a) PbSn after 1 min reflow at 210 °C (b) SnAg after 1 min reflow at 250 °C (c) PbSn after 20 min reflow at 210 °C (d) SnAg after 20 min at 250 °C (e) PbSn after 1 min reflow at 210 °C followed by 1000 hours annealing at 125 °C (f) SnAg after 1 min reflow at 250 °C followed by 1000 hours annealing at 150 °C

This TiW/NiV UBM is a modified UBM from Toshiba UBM for electroplated Sn/3.5Ag and Pb/63Sn bumps. The basic concept of this UBM is to use slower IMC growth rated Ni layer instead of Cu and slow down the interfacial reaction rate. And they reported that Ti 0.1 μm/ Ni 1 μm UBM structure showed good interface stability and bump shear strength using electroplated Pb/63Sn [34,35].

Fig.8 shows the cross-sectional images. With Pb/63Sn solder bump, the Ni-Sn IMC does not show any IMC spalling or detachment from the interface after 20 min reflow and 1000 hours aging. But the Ni-Sn IMC shows spalling during long time reflow with Sn/3.5Ag solder. Fig.9 (a), (b), and (c) shows the magnified images of Ni-Sn IMC spalling sequence with increasing reflow time. The remaining white layer after spalling is not the Ni but is detected as TiW layer by EDX analysis. This 0.2 μm TiW layer is expanded its thickness about to 0.8 μm and is gaining significant Sn content with increasing reflow time. The white TiW layer thickness is increasing with reflow time as shown in Fig.9(a), (b), and (c).

The Ni-Sn IMC morphology is normally not the smooth scallop-like shape but rather faceted images [36]. Our previous study revealed that the Ni-Sn IMC grains do not

have smooth surface morphology like Cu-Sn IMC because their atoms have relatively lower thermal movement energy compared to their high formation energy. Therefore, the Ni-Sn IMC spalling mechanism cannot be explained by the same mechanism of surface energy dominated Cu-Sn IMC spalling supposed by *Liu et al.* [37]. When the Ni-Sn IMC consumed all Ni from the UBM, the IMC meets the TiW layer which can not form any chemical bond with Sn and Ni. In the liquid state reflowing process, the molten solder fluids can detach the Ni-Sn IMC which does not have any more chemical bonding with the TiW layer.

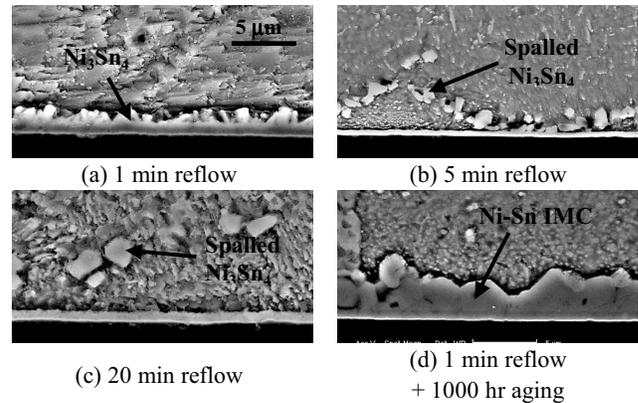
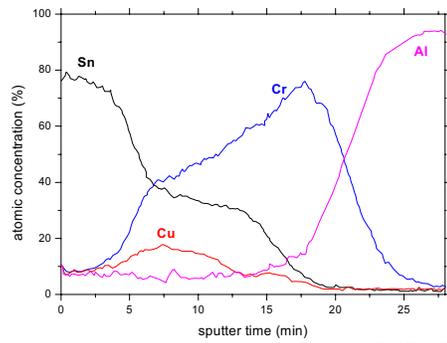


Fig. 9 Magnified SEM images of Sn/3.5Ag on TiW/NiV UBM

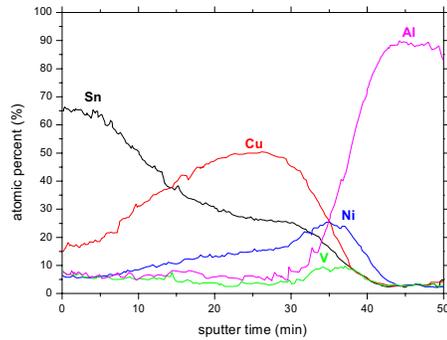
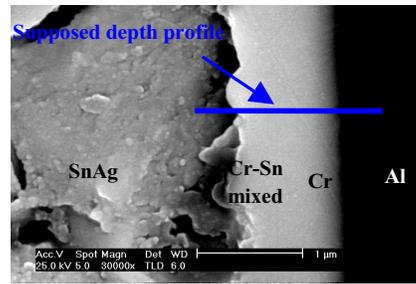
III-3. Diffusion Barrier Characteristics

The Cr, NiV, and TiW layers were used as direct contact material to the Al pad in the selected four UBMs. One of the main role of the UBM is to serve as an effective diffusion barrier between solder and chip pad. We investigated their diffusion behavior with Sn/3.5Ag after 1000 hours aged samples at 150 °C. In normal process, the reflow time should be controlled very strictly because the interface reaction develops dynamically in liquid state solder as discussed before. But the interconnection can easily experience high temperature exposure below the solder melting point during process and usage. In that reason, high temperature aged sample with highly reactive Sn/3.5Ag solder was chosen for diffusion barrier investigation.

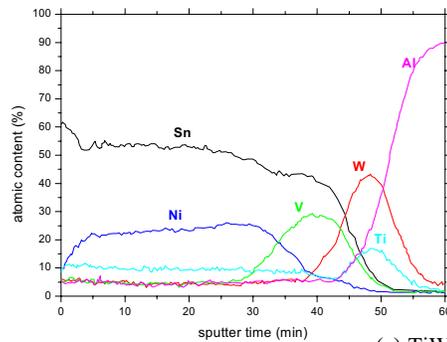
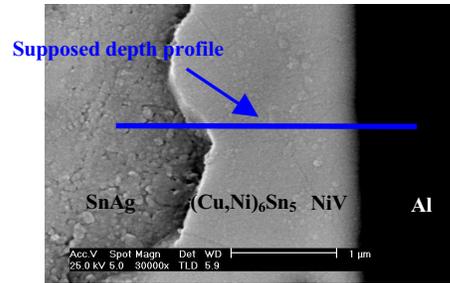
Fig. 10 represents the Auger depth analysis profile of 3 UBM systems. There was no severe Sn or Cu diffusion into Al side through the all barrier layers. The Cr/Cr-Cu/Cu UBM profile in Fig.10(a) shows the Sn diffusion into Cu depleted Cr-Cu layer after the Cu-Sn IMC spalling. The NiV/Cu UBM profile in Fig.10(b) indicates the NiV layer is remained between IMC and Al layer without severe change. The Ni is also detected in IMC region. There are some reports about ternary (Cu,Ni)₆Sn₅ IMC presence in the system containing these three components, and it is believed that the mixture of Cu-Sn and Ni-Sn bonds lowers the Gibbs free energy [38,39]. In the profile of TiW/NiV, Ni-Sn IMC and V-Sn mixed layers are separated. This shows that the Ni is consumed from Ni-V layer by IMC growth, but V remained its original position though Sn diffusion is reached that inner layer.



(a) Cr/Cr-Cu/Cu UBM with Sn/3.5Ag



(b) NiV/Cu UBM with Sn/3.5Ag



(c) TiW/NiV UBM with Sn/3.5Ag

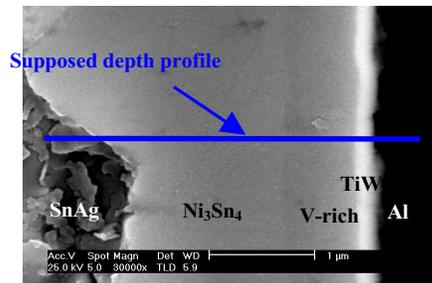


Fig.10 AES Depth Profiles of SnAg bumps after 1 min reflow followed by 1000 hours aging at 150 °C

Summary and Conclusion

- Pb-free Sn/3.5Ag alloy electroplating was successfully adopted to flip-chip bumping process using 4 different UBM systems on 6 inch wafer.
- Nowadays, Ni is preferred to Cu in UBM because it has a lower IMC growth rate. However, high internal stress effects of Ni should be seriously considered in the process design.
- Interface reaction in 4 UBMs with Pb/63Sn and Sn/3.5Ag solder bump was studied with reflow time and solid state aging time. The IMC growth rate is higher in Sn/3.5Ag than in Pb/63Sn. In solid state aging condition, the IMC surface does not have enough freedom to change its surface morphology and grows as a layered structure compared to the dynamic change of IMC morphology in liquid state reflow condition.
- In the UBM structure, if the final solder wettable Cu or Ni layer is thin (about 8000 Å), and their underneath layer is non solder wettable layer such as Cr or TiW, the Cu-Sn or Ni-Sn IMCs will spall-off from the interface through

long reflow times. This IMC spalling phenomenon appears in an earlier stage of reflow in Sn/3.5Ag compared to Pb/63Sn solder bumps.

- TiW, Cr, NiV layers in 4 UBMs successfully served as diffusion barriers in condition of 1000 hours aging at 150 °C with Sn/3.5Ag.
- This UBM study is designed to replace Cu plated UBM to only sputter layered UBM for electroplating bumping technology. All other 3 UBMs showed relatively good interface IMC adhesion with Pb/63Sn solder. The selection of thin sputtered layered UBM for Sn/3.5Ag solder remains some issues. The effects of thick IMC and IMC spalling on reliability should be studied furthermore.

Acknowledgements

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Study on Coined Solder Bumps on Micro-via PCBs

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Abstract

In this study, three solders, Sn-37Pb, Sn-3.5Ag, and Sn-3.8Ag-0.7Cu, were screen printed on both electroless Ni/Au and OSP finished micro-via PCBs. The pad opening size and pitch of micro-via PCB were 120 μm and 230 μm respectively. The diameter of the screen printed solder bumps was 150 μm and the height above the solder mask was 85 μm . After that, solder bumps were coined until 25 μm height by a newly developed coining machine with variables of pressure, temperature, and time.

The Sn-37Pb solder formed less amount of intermetallic compounds than all other Pb-Free solders on both electroless Ni/Au and OSP (Organic Solderability Preservatives) finished PCBs during solder reflows because of the lower Sn content of and lower reflow temperature. For OSP finish, fracture occurred 100% within the solder regardless reflow numbers. However, for Ni/Au finish, a brittle fracture at the Ni-Sn IMC layer or the interface between Ni-Sn intermetallic and P-rich layer was observed after several reflows.

The relation of coining load vs. height of coined solder bump showed three stage of coining deformation. Coining loads needed for same height deformation increased as applied coining rate increased. And the planarity of coined solder bump could be increased as the coining rate decreased. As the coining temperature increased, lower coining loads were needed.

Introduction

Flip chip technology becomes popular chip interconnection technology because of its excellent electrical performance, the smallest package size as chip size, and high I/Os handling capability compared with conventional wire bonding interconnection technology. Because of these advantages, flip chip technology is widely applied for various applications such as telecommunications, computers, appliances, and so on. However, for the flip chip technology to be cost competitive, it is necessary to use low cost organic substrates for flip chip assembly. When organic substrates are used for the high pin count flip chip assembly, substrate bending and warpage problems should be solved to guarantee good flip chip interconnection and high assembly yield [1]. One way to solve this problem is flip chip bumping on organic substrates pads, and then coining flip chip bumps to guarantee coplanarity of flip chip bump surface on which actual flip chip devices will be attached thereafter.

In this study, we have developed organic substrates solder flip chip bumping processes using a screen printing method, and then followed by coining process performed by specially designed coining machine with controlled gas environment, temperature, and strain rate.

Experimental procedures

The experimental procedure of screen printing solder bumping on micro-via PCB and coining process is shown in Fig 1.

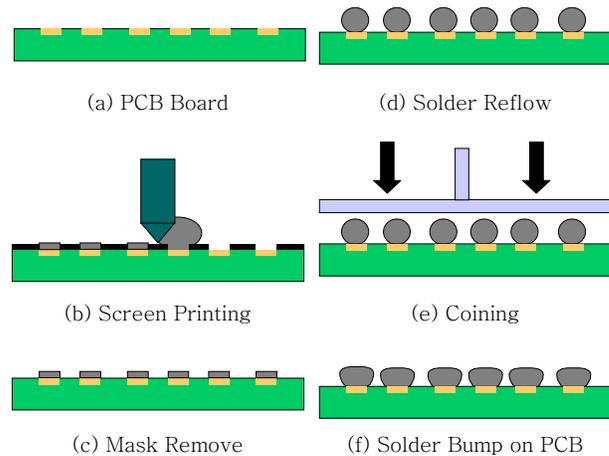


Fig. 1. Manufacturing process for producing coined solder bump on PCBs.

PCB surface finish type

For the successful application of solder bumped substrates, it is critical to understand the interaction between solder bumps and PCB surface finishes. The most common method of PCB metal surface finish is an electroless Ni/Au finish. However, because of its high production cost, recently, OSP (Organic Solderability Preservatives) finishes are commonly used in PCBs fabrication [2]. OSP process is the cheapest one among other preservative technologies and also fully ecological. Therefore, we have investigated the effects of the interfacial reaction between OSP and Ni/Au finishes, and three solders on the solder bump on PCBs reliability.

Bump formation and reflow condition

Three solders, Sn-37Pb, Sn-3.5Ag, and Sn-3.8Ag-0.7Cu, were stencil printed on both OSP and electroless Ni/Au finished micro-via PCBs. Reflow steps were classified in 3 stages: flux activation zone at 120°C and 150°C for 1 min,

dwelling zone at 210°C for Sn-37Pb solder and 250°C for lead-free solders respectively, and cooling zone for 90 seconds. 90sec dwell time was used for both solders. The pad opening size and pitch of micro-via PCB substrates were 120 μm and 230 μm respectively. The stencil printing was performed using an electroformed stencil mask with 180 μm diameter opening size and 75 μm thickness. The diameter of solder bumps after reflow was 150 μm and the height above the solder mask was 85 μm.

Coining process

Solder bumps were coined until 25 μm height in N₂ atmosphere by using a modified tension/compression tester as variables of pressure, temperature, and time. The variations of coining rate were 12, 6, 1.2, and 0.6 μm/sec and those of coining temperature were room temperature, 50, 100, 150, and 200 °C. Fig. 2 shows SEM images of solder bumps on PCB pads and coined solder bumps.

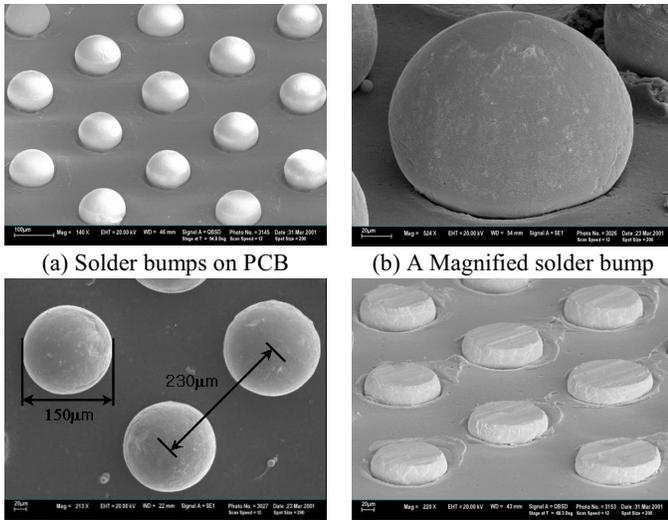


Fig. 2. SEM images of screen printed solder bumps on PCB and coined solder bumps.

Results and Discussion

PCB surface finishes/solder interface analysis

The cross-sections of solder bumps for 2 surface finishes/3 different solders combinations after first solder reflow are shown in Fig. 3. And IMC (Intermetallic compound) after fourth solder reflow are shown in Fig. 4. For the OSP finish, round shape Cu₆Sn₅ phases were observed at the Cu/solder interfaces. On the other hand, for electroless Ni/Au finish, it is interesting to find that there is a P rich layer formed at the Sn-Ni intermetallic and electroless Ni interface. Black lines below Sn-Ni IMC indicated P rich layer. During solder reflow, Sn diffused into E-Ni layer, forming IMC. As a result, P was expelled from the electroless Ni layer consumed for Ni-Sn IMC formation. The electroless Ni film contains about 9 wt. % P, and the P content in the P rich layer increases up to 20 wt. % after four reflow cycles. Besides, for electroless Ni/Au finish, the composition of IMC was dependent on the solder alloy composition. Polygonal shape Ni₃Sn₄ IMC was the primary IMC phase for three solders. But, according to the

EDX line scan and XRD analysis as shown Fig. 5 and Fig. 6, a ternary composition of IMC which has (Ni,Cu)₃Sn structure was formed in SnAgCu case.

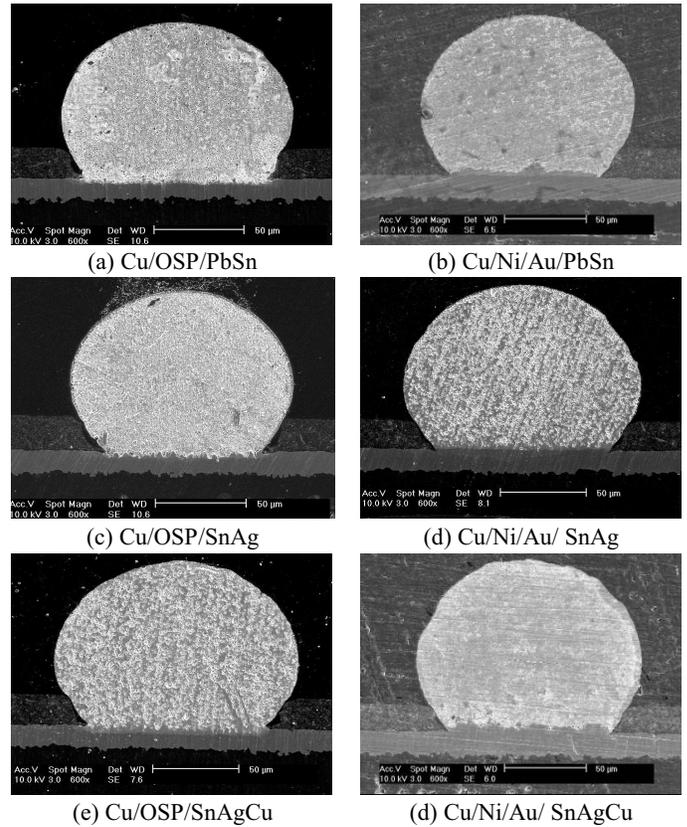


Fig. 3. SEM cross-sectional images of Sn-37Pb, Sn-3.5Ag, and Sn-3.8Ag-0.7Cu solder bumps on different PCB surface finishes after one reflow at 210°C and 250°C.

The elemental cross-sectional analysis of Ni/Au surface finish and SnAgCu solder interface after fourth solder reflows shows that copper was detected in IMC layer. From the XRD analysis, the Ni₃Sn₄ IMC peaks in SnAgCu solder shifted toward lower angle than those of PbSn and SnAg solders. Lattice parameters of IMC of SnAgCu solder probably increase due to substitutionally incorporated copper atoms, because the atomic size of copper is bigger than that of nickel.

The IMC spalling away from the interface results from the faster dissolution rate between SnAg solder and electroless Ni because of higher reflow temperature and Sn content than PbSn solder. However, the ternary (Ni,Cu)₃Sn IMC adhered well to the P rich layer in spite of the faster dissolution rate in lead free solders.

Bump shear test

The average bump shear strength measured at each PCB surface finishes and solders were shown Fig. 7. Bump shear strength values of the OSP finish are relatively higher than those of Ni/Au finish. For OSP finish, fracture occurred 100% within the solder regardless reflow numbers because of thick Cu thickness and solder mask height. Their fracture mode was the Mode I as shown in Fig. 8. In case of the cohesive failure at solder bumps, lead free solders showed higher value than

PbSn solder because bump shear strength value depend on only solder bump hardness. The hardness value of lead free solders was higher than that of PbSn solder [3]. However, for Ni/Au finish, a brittle fracture at the IMC layer (Mode II) or the interface between Ni-Sn intermetallic and P-rich layer (Mode III) was observed after several reflows.

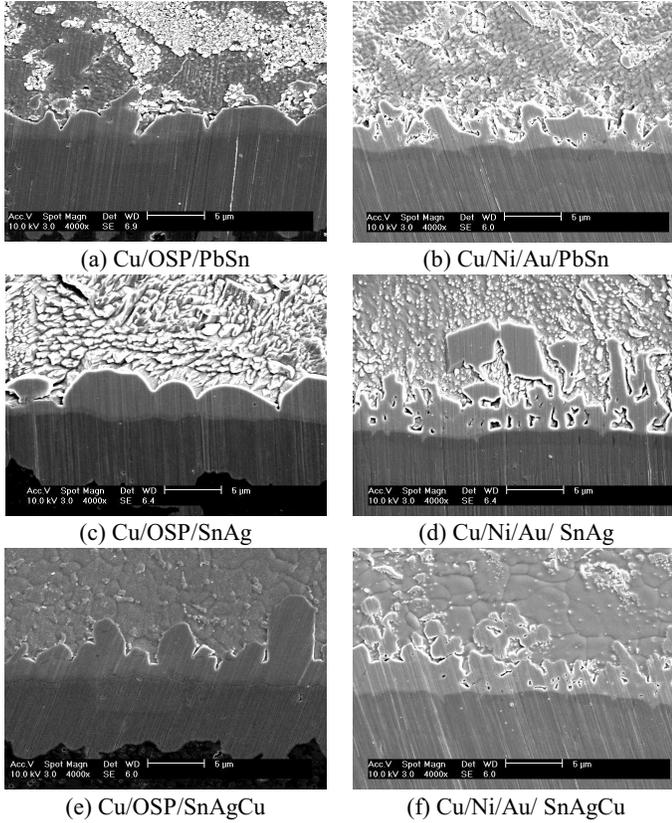


Fig. 4. Cross-sectional SEM images after four reflows at various PCB surface finishes/solder interface systems.

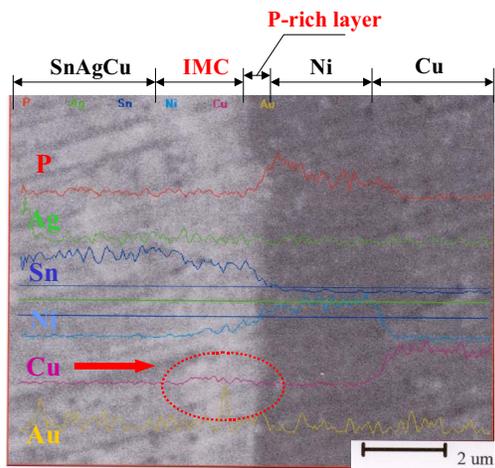


Fig. 5. Elemental EDS Line profile for cross section of Ni/Au/SnAgCu solder after 4 reflow.

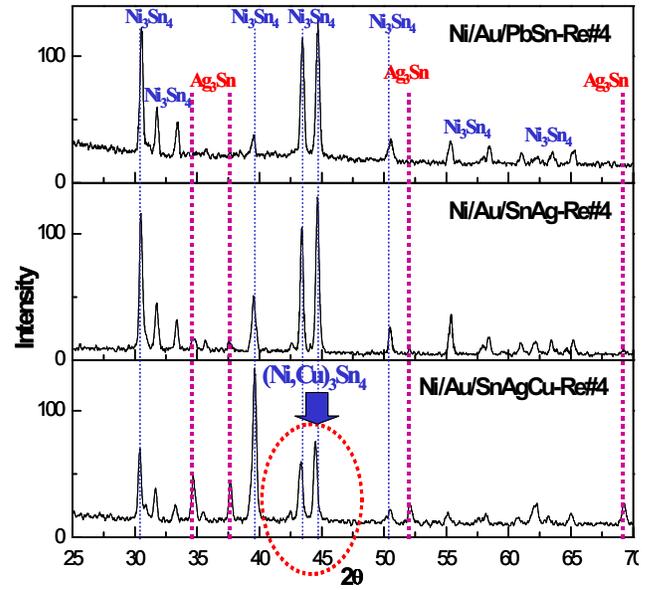
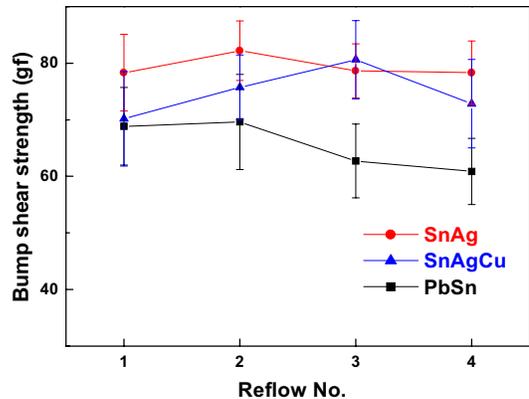
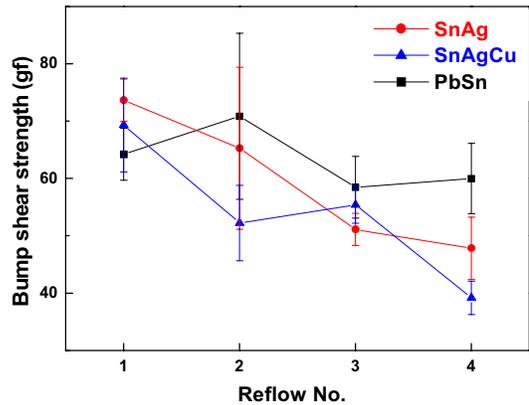


Fig. 6. XRD analysis of IMCs between Ni/Au finish and various solders.



(a) Solder bumps on OSP finish PCB



(b) Solder bumps on Ni/Au finish PCB

Fig. 7. Bump shear strength variation of PbSn, SnAg, and SnAgCu solder bumps as PCB surfaces finishes and numbers of reflows.

The fracture occurred at the solder bump itself after one reflow cycle, however, a failure occurred partly at the IMC layer or the solder and the IMC/P rich layer interfaces as the numbers of solder reflows increase. Because of faster IMC and thicker P rich layer formation for lead free solder, the possibility of brittle fracture increased resulting in lower bump shear strength of lead free solder cases after several reflow times. Fracture modes after bump shear test at each surface finishes and solders with multiple reflow were shown in Table I.

Table I. Fracture modes of two types of PCB surface finishes and solders as multiple numbers of reflows.

Sn-37Pb solder bumps				
Reflow No.	1	2	3	4
OSP	I	I	I	I
Ni/Au	I	I	IV	IV (10%) V (90%)
Sn-3.5Ag solder bumps				
OSP	I	I	I	I
Ni/Au	I	II (92%) I (8%)	III (95%) V (5%)	V (78%) III (22%)
Sn-3.8Ag-0.7Cu solder bumps				
OSP	I	I	I	I
Ni/Au	I	II (90%) III (10%)	II (94%) III (6%)	V (90%) VI (10%)

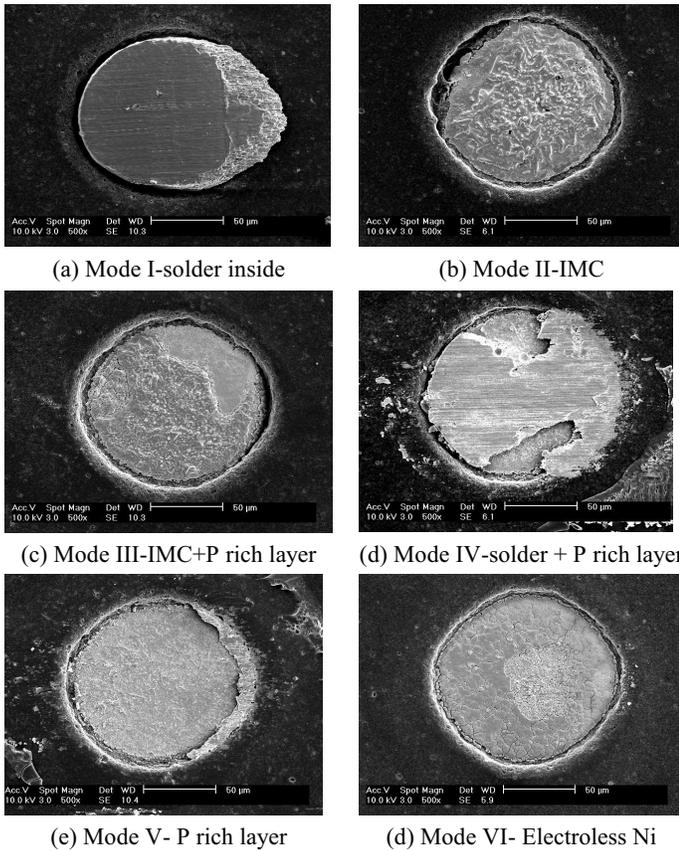


Fig. 8. Fracture modes after bump shear test.

Coining I – Load vs coining height

Fig. 9 shows the SEM image of coined PbSn solder bump on PCB as various coining load. Fig. 10 shows the relationship between load and coining height at various solders. It is found that the load vs. height plot of coined solder bump shows three stage of coining deformation. The primary stage is characterized by remained elastic effect at initial deformation. The secondary stage of coining deformation is characterized by yield strength for plastic deformation. The final rapid increased stage, more loads needed for same height deformation because not only compressive stress but also shear stress interacts within solder bumps. Since the Young’s modulus and yield strength value of lead free solders were higher than PbSn solder [4], the load needed for same height deformation at lead free solders were higher than PbSn solder in primary and final stage. However, although the yield strength value of PbSn solder was lower than lead free solders, the load needed for same height deformation at PbSn solder was higher than lead free solders in the secondary stage. In practice, the volume change of solders was considerable in secondary stage. It seems that lead free solders needed lower load during compress to a specific volume, because the density of lead free solder was lower value than PbSn solder [5].

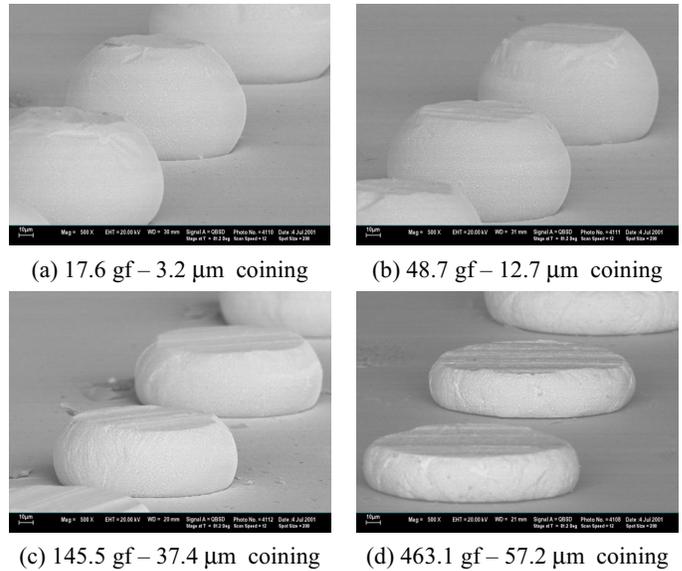


Fig. 9. SEM images of coined PbSn solder bumps at various coining loads.

The metal lines and solder mask of PCB were not damaged during solder coining process. Fig. 11 shows the cross-sectional SEM images of coined PbSn solder bump on OSP finished PCB. Any damages in PCB were not observed after coining process until 25 µm height.

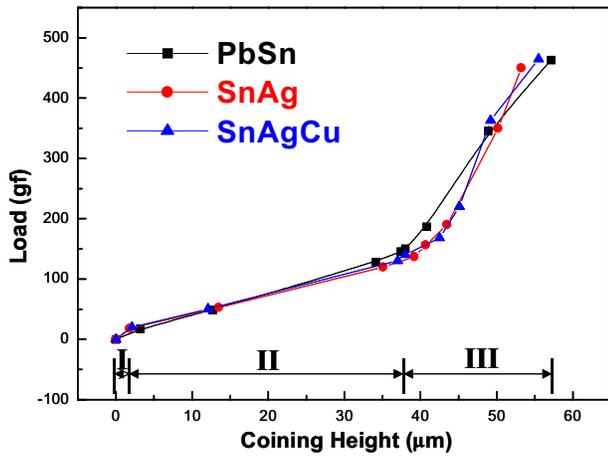


Fig. 10. Coining load variations of PbSn, SnAg, and SnAgCu solder bumps as coining height.

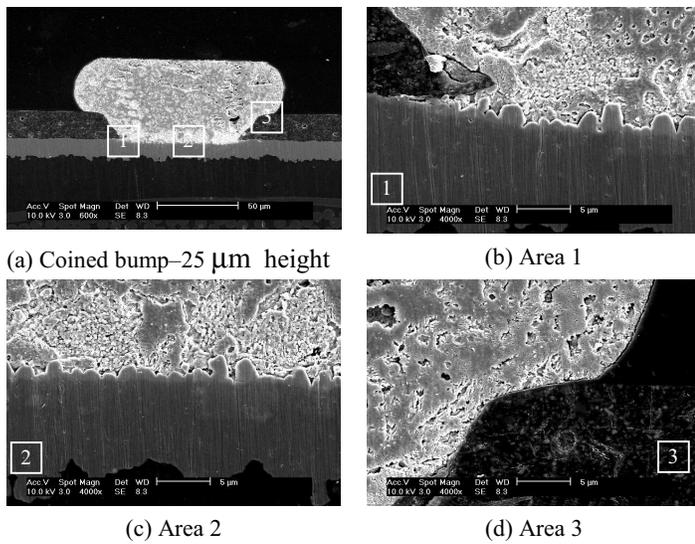


Fig. 11. Cross-sectional SEM images of a coined PbSn solder bump on OSP finished PCB

Coining II – Effect of coining rate and temperature

Fig. 12 shows how coining load as a function of applied coining rate and environmental temperature for same height deformation until 25 μm height.

When the solders were deformed at rapid deformation state, there were work hardening effects on solders. Therefore, loads needed for same height deformation increased as the applied coining rate increased. Similar result was reported in the tensile stress experiment of PbSn solder [6]. The total strain increased and yield strength decreased as the strain rate decreased at room temperature.

The effect of coining rates on coining loads at 100 °C was shown in Fig. 12 (b). Coining loads increased, as the applied coining rate increased as room temperature process. However, at high temperature coning process, solder bumps were deformed with lower loads than room temperature at the same coining rate regardless of kinds of solder.

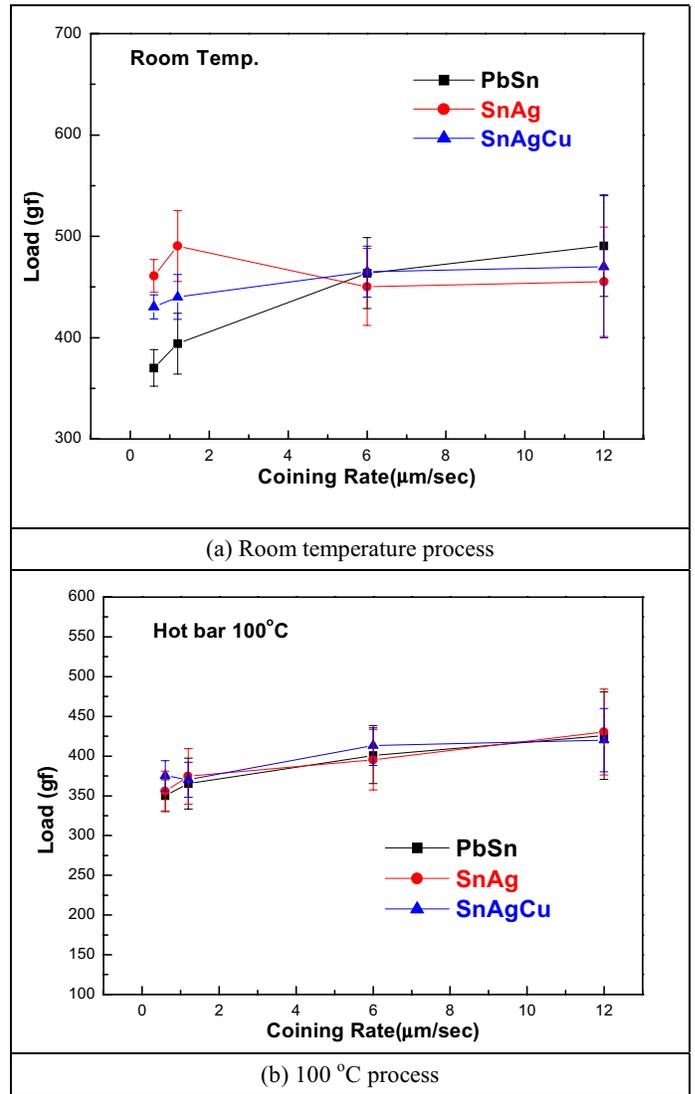


Fig. 12. Coining loads of PbSn, SnAg, and SnAgCu solder bumps versus coining rates at room temperature and 100 °C.

Conclusions

Screen printed solder bumps with 150 μm diameter and the 230 μm pitch were successfully demonstrated by using an electroformed print mask. And it was found that OSP finished PCB was a better choice for solders on PCB in terms of mechanical reliability.

Solder bumps were successfully coined until 25 μm height by using a modified tension/compression tester as variables of pressure, temperature, and time.

The load vs. height plot of coined solder bump shows three stage of coining deformation. As a results of comparison with various solders which has different Young's modulus and yield strength value, it seems that coining loads were affected not only by Young's modulus and yield strength but also by more complex factors such as density and ductility of solders.

Values of coining loads for the same height deformation strongly depend on coining rate and coining temperature. Loads needed for same height deformation increase, as applied coining rates increase. At high temperature coning process, solder bumps were deformed with lower load than

room temperature at the same coining rate regardless of kinds of solder.

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Fluxing For Flip Chip Assembly - Effect Of Bump Damage

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Abstract

Solder bumps on flip chips could arrive at the manufacturing floor with prior damage. While bumps with insufficient solder volume may not solder well even if adequately fluxed, the bumps that are flattened during damage are also of concern for fluxing. Good assembly yields will depend on whether these bumps are fluxed adequately and whether the collapse offered by the substrate design is sufficient to bring the damaged bumps in contact with their target pads. The former depends on the flux application method and the latter depends on the pad design and the solder alloy. When assembled on the same substrates, lead-free solder joints have been shown to exhibit less collapse than eutectic tin-lead solder. Therefore, a damaged lead-free solder joint may not solder well even if it is adequately fluxed. The sensitivity of four flux application methods to bump damage is described in this paper. Solder bumps on flip chips were systematically damaged by flattening them to an extent of 40-45 μm . These damaged chips were then assembled using four different fluxing techniques: dip fluxing, stencil printing, flux jetting and no-flow encapsulation. Soldering of three alloys, eutectic tin-lead, Sn-Ag-Cu (LF2) and Sn-Ag-Cu-In (LF1) was studied. Assembly was followed by X-ray inspection, micro-sectioning and electrical testing. As expected, dip fluxing proved to be sensitive to bump damage. Defects were observed with both tin-lead and LF2 chips with the least thickness of flux. Damaged LF1 bumps soldered very well even with a limited amount of flux. Both stencil printing and flux jetting were insensitive to bump damage and resulted in good soldering for all three alloys. The no-flow encapsulation process gave good soldering with both tin-lead and LF1 chips when used with the appropriate reflow profile. Since the reflow encapsulant material is designed for use with tin-lead, the encapsulant gelled before soldering of the LF2 bumps occurred.

Introduction

The statistics of bump height variations on flip chips due to the bumping process are reasonably well known. Thus, for a bump height variation of about 2-5%, one in every 1000 chips will have a bump that is shorter than the average by about 1.0 mil. These variations are normally considered in the development of the assembly process. However, flip chips that arrive at the manufacturing floor could have sustained damage to their solder bumps during subsequent processes such as dicing and handling and these variations are harder to evaluate. The bumps that lack enough solder volume may not solder well even if adequately fluxed. However, it often happens that the bumps are only flattened a bit and these bumps have enough solder to form a reliable interconnection. From an

assembly yield perspective, the concern is whether these damaged bumps will give reliable soldering.

Of course, this will depend on whether these bumps are fluxed adequately and whether the collapse offered by the substrate design is sufficient to bring the damaged bumps in contact with their target pads. The first question is related to the fluxing method. In a conventional flip chip assembly process, fluxing is achieved by dipping the chip in a thin film of flux as shown in Figure 1. In this process, the amount of flux on each bump is set by how tall the bump is relative to the tallest ones. Obviously, this limits the amount of flux in the place where it is most needed. Alternative fluxing methods such as stencil printing or flux jetting may be used to work around this problem. The second question is related to whether the substrate design offers enough collapse for the solder alloy that is used. Published literature shows that lead-free solder bumps do not collapse as much as eutectic tin-lead bumps under similar assembly conditions [1]. It has also been shown that the lead-free alloys may be more sensitive to the amount of flux. Therefore, sensitivity to bump damage varies with the solder alloy that is used.

This paper discusses the sensitivity of four fluxing methods to bump damage in an effort to qualitatively

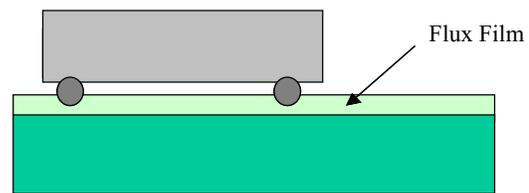


Figure 1. Dip Fluxing

understand the relative merits and demerits of these methods from an assembly yield standpoint. Since the sensitivity to bump damage depends on the solder alloy that is used, three solder alloys are also considered in this study.

Experiment

This study used an 88 I/O, perimeter array, nitride passivated chip, shown in Figure 2, on 62 mil thick FR-4 substrates with Ni-Au coated copper pads. The traces were 3 x 7 mils and this substrate design tends to give strong solder joint collapse. The typical distance between the Under Bump Metallurgy (UBM) and the top of the pad is about 2 mils, with typical flux levels. Since the typical bump height on the chip before assembly is about 4.5 mils, the collapse amounts to about 2.5 mils.

The bumps on the chips were first damaged systematically by applying 1500 grams of force as the chips were held against a metal shim in a placement machine. Figure 3 shows a

damaged chip. Subsequently the solder bumps on these chips were measured on a white light interferometer. Upon measurement, the damage was found to be about 40-45 μm for all the three alloys. Three solder alloys were considered, eutectic Sn-Pb, Sn-Ag-Cu (LF2) and the Sn-Ag-Cu-In (LF1). Appropriate reflow profiles were used and the details are shown in Table 1. Four flux application methods were considered, flux dipping, stencil printing, flux jetting and no-flow encapsulation.

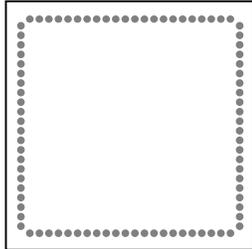


Figure 2. Chip Layout

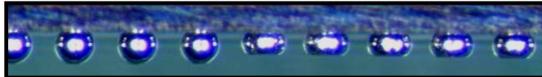


Figure 3. Damaged Bumps

Alloy	Alloy Melting Point ($^{\circ}\text{C}$)	Peak Temperature ($^{\circ}\text{C}$)	Time Above Liquidus (sec)
Tin-Lead	183	220	66
LF2	217	238	54
LF1	197	227	68

Table 1. Reflow Profiles Used in the Experiment

Flux Dipping

As said earlier, in flux dipping, the amount of flux on a given bump on a chip is set by the bump height distribution. This restricts the amount of flux on the shortest bumps, where it is most needed. Flux dipping happens in an expensive placement machine and it can slow down the assembly process by as much as 15%. However, it does have the advantage of limiting flux (and flux residues) to the area around the solder bumps.

In this study, Flux A was used for dip fluxing. Assembly of the tin-lead chips was done using three different flux thicknesses, 1.0, 1.5 and 2.0 mils, as measured on the thin film applicator. Since it was known from previous work that lead free alloys would need more flux in order to solder well, thicknesses of 1.5, 2.0 and 2.5 mils were used for LF2 and LF1.

Stencil Printing

In stencil printing, the flux is deposited onto the substrate pads before the chip is placed. Thus, the amount of flux does not depend on the bump height distribution but rather on the stencil design. In the present study, the stencil was about 2 mil thick and it is therefore reasonable to expect a flux thickness

of at least 2 mils, if not more. While large amounts of flux may be good from an assembly yield perspective, it may not be good for reliability because of the amount of flux residues that will be left behind. Stencil design and the stencil printing process are well understood and this is a huge advantage. Though stencil printing of flux may not be compatible with traditional SMT processes, it takes the fluxing process out of the placement machine. Tacky flux B was used in this experiment on a 2 mil thick, laser cut, stainless steel stencil with 3x6 mil apertures.

Flux Jetting

Flux jetting is a relatively new method of dispensing liquid fluxes. This is much like flux spraying, however, it offers greater control over the amount and location of flux. Like an underfill dispenser, a fine nozzle is used to dispense the flux. However, a coaxial air supply is additionally used to make an aerosol of the flux and the flux is deposited in a fine layer that is typically less than 1 mil thick. Liquid fluxes are mostly alcohol based and thus have a tendency to volatilize. This is an important concern for flip chip assembly yield because the flux should not volatilize in the reflow oven before soldering can happen. Further, if multiple sites are being fluxed, the site that received the flux first may volatilize before the chip is placed on that site. Flux jetting, however, is attractive because it takes the fluxing operation out of the placement machine. In the present study, flux jetting was done on an underfill dispenser equipped with a flux-jet head and the liquid flux C for assembly.

No-Flow Encapsulation

In this process, the underfill is dispensed onto the substrate before the chip is placed. The underfill not only acts as the flux but also is cured at the end of the reflow soldering cycle. This process eliminates the underfilling and curing steps [2]. However, the chip must still be held against the underfill in the placement machine with sufficient force until the underfill is forced out and wets the edges of the chip. This means that the most expensive machine on the line may be slowed down. From an assembly yield perspective, the bumps in this process are totally covered with the flux underfill and reliable soldering will happen as long as the bumps can make contact to the substrate pads.

Results and Discussion

Flux Dipping

For the eutectic tin-lead chips, assembly with a flux thickness of 1.0 mil gave defects. While the chips were electrically continuous, micro-sectioning of these chips revealed poor soldering as shown in Figure 4. However, undamaged bumps in the same chip soldered quite well, as shown in Figure 5. When these chips were removed off the substrate manually, there was no or little solder left on the pads with the damaged bumps. Evidently, these bumps were not fluxed at all and yet the chips were electrically continuous. This is because weak mechanical joints are formed as the molten solder is forced against the readily wetted Ni-Au surface. With higher flux thicknesses, 1.5 and 2.0 mils, the

damaged bumps soldered well. However, there was an observable effect of flux thickness on the collapse as measured by the standoff between the pad and the UBM as shown in Table 2.

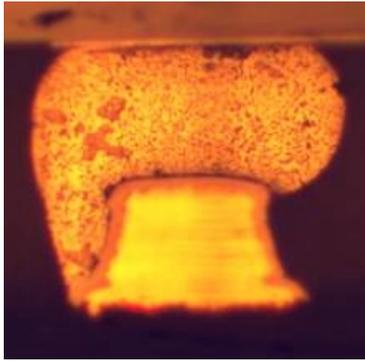


Figure 4. Poor Soldering of a Damaged Tin-Lead Bump With 1.0 mil Thick Flux

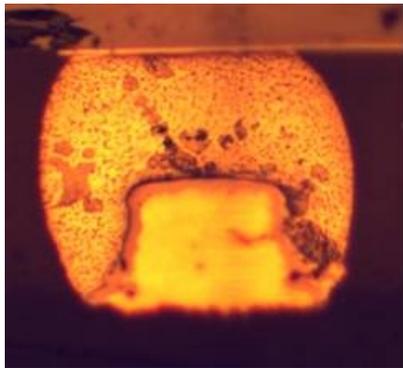


Figure 5. Good Soldering of an Undamaged Tin-Lead Bump With 1.0 mil Thick Flux

Alloy	Flux Thickness (mils)	Standoff (mils)
Tin-Lead	1	2.5
Tin-Lead	1.5	2.2
Tin-Lead	2	2
LF2	1.5	2.5
LF2	2	2.35
LF2	2.5	2.2
LF1	1.5	2
LF1	2	2
LF1	2.5	2

Table 2. Standoff Obtained for Different Alloys With Dip Fluxing

With the LF2, the least thickness of flux, 1.5 mils, resulted in defects. Unlike the damaged tin-lead bumps dipped in 1.0 mil thick flux, the damaged LF2 bumps were fluxed with some flux in a 1.5 mil thick flux film. However, it was not sufficient enough to form a good solder joint (Figure 6). Similar to the tin-lead alloy, the undamaged bumps in the same chip soldered quite well. With higher thicknesses of flux, even the damaged bumps soldered well. However, there was a notable dependence of collapse on flux thickness as measured

by the standoff between the pad and the UBM (Table 2). This dependence is sure to have an effect on assembly reliability [3]. With the LF1, good soldering was achieved with all flux thicknesses (Figure 7). There was no obvious effect of bump damage on soldering (Table 2).

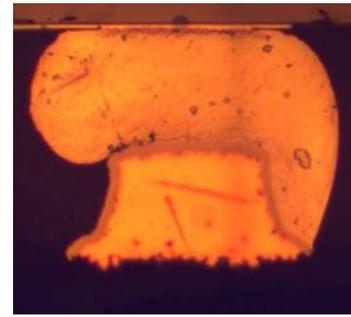


Figure 6. Poor Soldering of a Damaged LF2 Bump With 1.5 mil Thick Flux

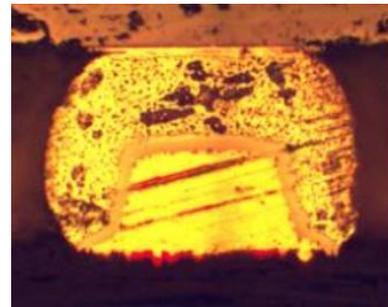


Figure 7. Good Soldering of a Damaged LF1 Bump With 1.5 mil Thick Flux

Stencil Printing

With all the alloys, no obvious effect of bump damage was observed when assembled using the stencil printing process (Figure 8). It is quite likely that the damaged bumps came in contact with the flux on the substrate during placement itself because the flux deposits on the pads tend to be about 2.0 mil tall.

While good soldering of damaged bumps using flux printing is encouraging from an assembly yield point-of-view, there are concerns about flux thickness variations from a process control viewpoint. Bridging of LF2 solder joints was observed with stencil printing. Further, issues such as integrating flux printing with the standard SMT process, stencil wear and cleaning will have to be addressed.

Flux Jetting

With all the three alloys, damaged bumps soldered well when assembled by flux jetting (Figure 9). In all the cases, visual inspection was done to ensure that all the pads were covered with flux. The level of control over the application of flux using flux jetting was by no means perfect at the time of this experiment. If indeed good soldering could be achieved for damaged chips with the current level of control, better control can only make flux jetting a more attractive option. Of

course, knowledge of the reliability of flip chips assembled with flux jetting is very limited at present. There are a number of no-clean liquid fluxes that also need to be evaluated for this process.

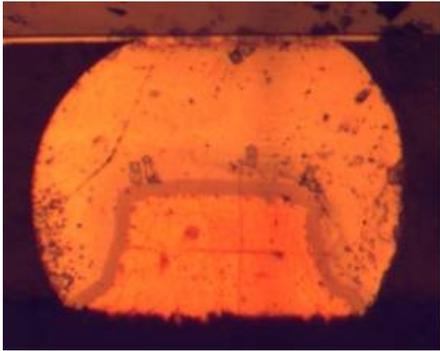


Figure 8. Good Soldering of a Damaged LF2 Bump With Stencil Printing

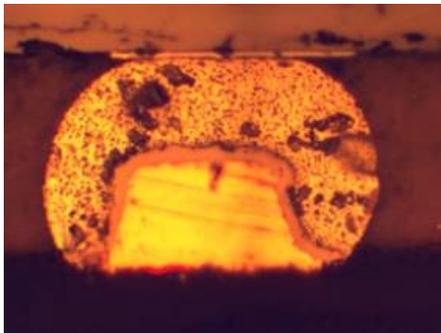


Figure 9. Good Soldering of a Damaged LF1 Bump With Flux Jetting

No-flow Encapsulation

For the tin-lead and LF1 chips, the no-flow encapsulation process proved to be insensitive to bump damage (Figure 10). The no-flow encapsulant D is primarily designed for eutectic tin-lead applications. However, when used with the appropriate reflow profile for the LF1, it resulted in good soldering of the damaged bumps as well. However, with the hotter LF2 profile, it gelled before the peak reflow temperature was reached and resulted in poor soldering of the LF2 (Figure 11).

Conclusions

The sensitivity of different flux application techniques to bump damage was evaluated. As expected, flux dipping proved to be sensitive to bump damage. Eutectic tin-lead bumps were less sensitive to flux thickness than LF2 bumps; a higher thickness of flux (1.5 mils) was sufficient to overcome bump damage. There was notable effect of flux thickness on soldering of LF2 chips. An increase in flux thickness from 1.5 mils to 2.5 mils resulted in a decrease in standoff from 2.5 mils to 2.0 mils with the hotter reflow profile. Damaged LF1 chips gave good soldering with all flux thicknesses.

Both stencil printing and flux jetting were insensitive to bump damage and resulted in good soldering for all the three

alloys. Bridging of LF2 solder joints was observed with stencil printing. Flux jetting promises to be a viable option, particularly because it limits the amount of flux applied to the substrate. However, the reliability of flip chips assembled by the flux jetting process needs to be studied. Better control over the process is also possible. The no-flow encapsulation process gave good soldering with both tin-lead and LF1 chips when used with the appropriate reflow profile. Since the material is intended for use with tin-lead, the encapsulant gelled before reaching the reflow temperature for LF2.

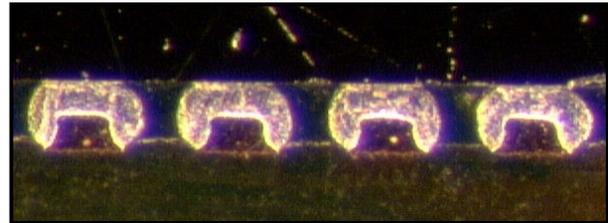


Figure 10. Good Soldering of a Damaged LF1 Bumps With No-Flow Encapsulation

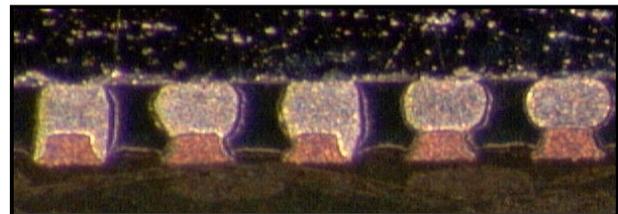


Figure 11. Poor Soldering of LF2 Chip With No-Flow Encapsulation Due to Underfill Gelling

Acknowledgments

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