Session C-2

Core – Electronics Materials(2)

A Method of Improving Dielectric Constant and Adhesion Strength of Methyl Silsesquioxane by Using a NH_3 Plasma (*Invited*)
Yong Tae KIM ; Korea Institute of Science and Technology, Korea

Thermal and Adhesive Properties of Cu Interconnect Deposited by Electroless Plating
Jung Sik KIM, University of Seoul, Korea

Electrical Characterization of Silicided CMOS Devices for Embedded DRAM and Logic with Ti and TiN Capping Layers
Jong Chae KIM, Yeong Cheol KIM, Hwa Il SEO, Korea University of Technology and Education, Korea

Percolation-Controlled Electronic and Optical Properties of Microcrystalline Silicon Films
K. SHIMAKAWA, Gifu University, Japan

Carbon Nanotube Synthesis Using Arc Discharges
Hirofumi TAKIKAWA, Tateki SAKAKIBARA, Toyohashi University of Technology, Japan

Thermal and Adhesive Properties of Cu Interconnect Deposited by Electroless Plating

J. S. Kim
Department of Materials Science and Engineering
University of Seoul, Seoul 130-743, Korea
e-mail: jskim@uoscc.uos.ac.kr

Abstract

In the present study, the adhesion and thermal property of the electroless-deposited Cu thin film were investigated. The multilayered structure of Cu/TaN/Si was fabricated by electroless-depositing the Cu thin layer on the TaN diffusion barrier which was deposited by MOCVD on the Si substrate. Crystallization and agglomeration of the electroless-deposited Cu film occurred through annealing at H_2 atmosphere and resulted in the decrease of film resistance. Thermal stability of Cu/TaN/Si system was maintained up to the annealing temperature of 600°C in H_2 atmosphere above which the intermediate compound of Cu-Si was formed through diffusion into the TaN layer. The adhesion of the electroless-deposited Cu film was compared with other deposition methods of thermal evaporation and sputtering. The scratch test showed that the adhesion of electroless plated Cu film on TaN was better than those of sputtered Cu film and evaporated Cu film.

1. Introduction

For future ICs, copper is being considered as an alternative to Al alloys [1-2] because of its low bulk elecrical resistivity and improved electromigration performance. Deposition processes of Cu metallization have been intensively studied through PVD, CVD, laser reflow, electroplating and electroless deposition, etc. According to most reported results, physical vapor deposition of Cu showed poor step coverage, while the chemical vapor deposition showed good step coverage, but somewhat showed uncertain reliability problems such as impurities, high resistivity with different processing condition. The electrochemical method of electroplating and electroless deposition has been recently considered as the prominent technique of Cu metallization owing to the development of chemical-mechanical polishing (CMP) and damascene processes in the semiconductor processing. The electroplating and electroless deposition produce high-quality Cu filling of the high-aspect ratio via contacts and lines[3-4]. Also, they shows low electrical resistivity (~1.7μΩ·cm) and excellent electromigration reliability[5].

In the present study, the adhesion and thermal properties of the electroless-deposited Cu thin film were investigated. The multilayered structure of Cu/TaN/Si was fabricated by electroless-depositing the Cu thin layer on the TaN diffusion barrier. Adhesion property of the electroless-deposited Cu film was evaluated by the scratch test. Also, the annealed Cu/TaN/Si system was analysed for the thermal stability and electrical property by using a 4-point probe, SEM, XRD and AES.

2. Experimental Procedure

The substrates used in the present study were p-type (100) Si wafers with resistivity of 1-100 Ω·cm. The Si wafer surface was cleaned by 5% HF solution and Ar-plasma etching process in order to remove the native oxide layer on a Si substrate prior to the deposition of diffusion barrier, TaN. The MOCVD TaN films were deposited using pentakis-methyl-amino-tantalum (PEMAT) as a precursor which was carried out by Ar gas into a reaction chamber at 1-torr. The temperature of substrate was varied from 250°C to 350°C in order to find out the appropriate condition for film deposition.

Next, electroless deposition of Cu on the TaN diffusion barrier was carried out by dipping in the solution bath which consists of copper sulfate, formaldehyde and minor additives. An activation treatment was performed with a dilute solution of $PdCl_2$ prior to Cu-electroless deposition, and the pH of the solution bath was controlled by adding the NaOH solution. The Si/TaN/Cu specimens were annealed at temperatures ranging from 350 to 800°C for 30min in a H_2 reduction atmosphere. Adhesion of the Cu-film was evaluated by the scratch test (CSEM-Revetest). The test was conducted by drawing a stylus with diamond tip of 200 μm radius over a Cu-film under increasing vertical loads. Signals of acoustic emission and friction coefficient (μ) were detected.

The film thickness and surface morphology were measured by SEM. Resistivity was measured by a four-point probe. Analyses on the thermal stability for the Si/TaN/Cu system were carried out by XRD and AES. A glancing angle x-ray diffraction spectra was obtained by using a Rigaku X-ray diffractometer with Cu-Kα radiation, 40kV and 100mA.

3. Results and Discussions

Fig. 1 shows SEM surface images of electroless-Cu for Cu/TaN/Si specimen (a) as-deposited, (b) annealed at 450°C, and (c) 650° in H_2 atmosphere. As the annealing temperature increases, the evidence for agglomeration of the electroless-Cu appears as white spots. Especially, at 650°C the Cu film was partially destroyed by severe agglomeration of Cu (irregularly-shaped white particles). Fig. 2 shows the XRD spectra for Cu/TaN/Si specimens annealed at temperatures from 350°C to 650°C in H_2. Increased (111) and (200) peaks of annealed-Cu film indicate the evidence of Cu crystallization taken placed as annealing temperature increases. Up to 600°C of annealing temperature, Cu and TaN peaks appeared. However, intermediate compounds of Cu-Si system such as Cu_4Si and Cu_3Si were formed at 650°C, indicating the occurrence of severe inter-diffusion of Cu and Si, and the limit of TaN film as a diffusion barrier to be around 650°C.

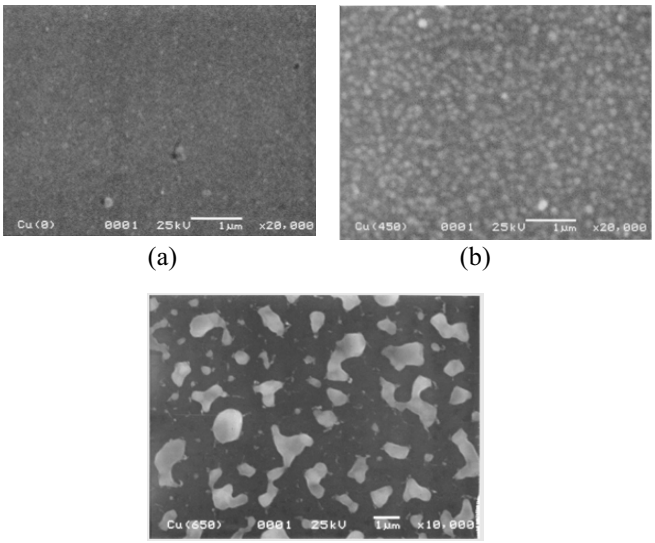


Fig.1. SEM micrographs of surface morphology for the electroless Cu film in Cu/TaN/Si system annealed in H_2 atmosphere. (a) as-deposited, (b) 450°C, and (c) 650°C

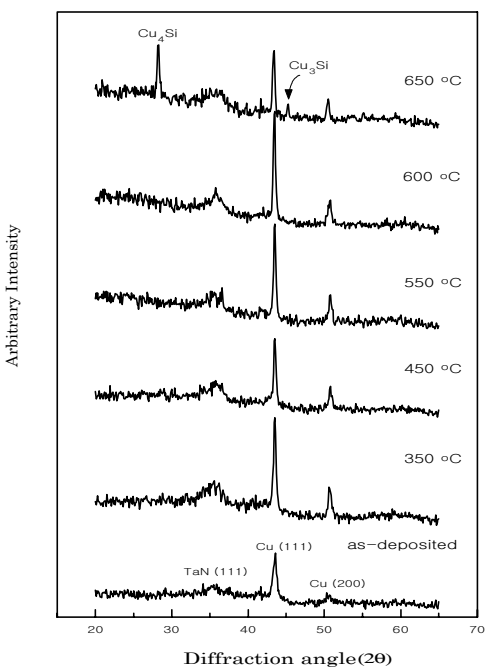


Fig.2. XRD spectra of Cu/TaN/Si system according to annealing temperature in hydrogen ambient.

In order to inspect interfacial reaction of Cu/TaN/Si system with annealing temperature in detail, the depth profile of AES was carried out. Fig. 3 shows the results of AES analysis for specimens annealed at 350, 550, 650 °C. In case of specimens annealed at 350°C and 550°C, depth profiles are similar each other and have no intermixing evidence at interfaces of Cu/TaN and TaN/Si. However, in the case of specimen annealed at 650°C, intermixing at interfaces among Cu/TaN and TaN/Si took placed. Cu penetrated into the TaN layer to reach Si-substrate and TaN layer was observed even at surface. This result agrees well with that of XRD spectra.. The temperature dependence of diffusivity is expressed by the Arrhenius relationship of $D=D_o\exp(-Q/kT)$, where D_o is the proportional factor, Q is the activation energy for diffusion, k is the Boltzmann constant, and T is temperature. The Q (eV) and Do (cm^2/sec) values caculated from the results of AES depth profiles in the range of 650°C~800°C are shown in Fig. 4. The detailed explanation for calculating D_o and Q are written elsewhere[6].

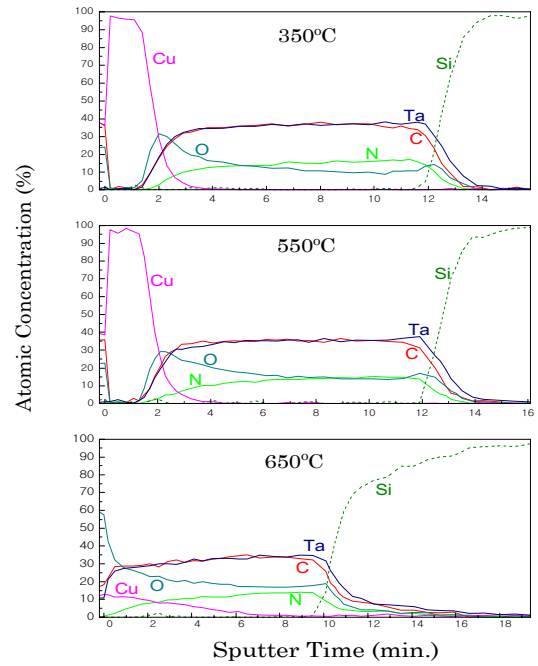


Fig.3. AES depth profiles for Cu/TaN/Si systems annealed at temperatures of 350～650℃ in H_2 atmosphere.

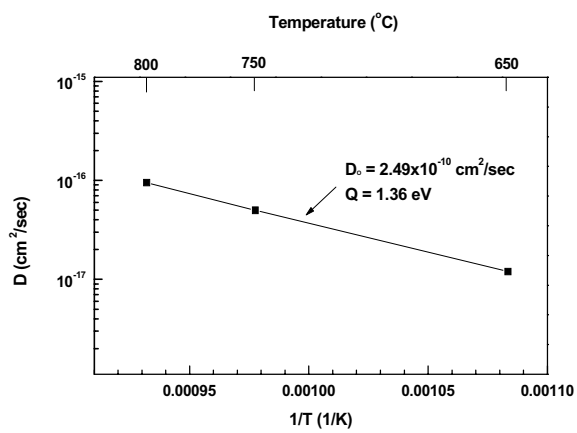


Fig.4. Diffusion coefficients of Cu in TaN barrier at temperatures ranging from 650°C to 800°C

Fig. 5 shows the resistivity of the Cu/TaN/Si system measured by a 4-point probe upon annealing in H_2 atmosphere for 30min. Specimens annealed through 450°C~600°C show resistivity less than the as-deposited one, which indicates an evidence on the crystallization and grain growth of Cu film. Specimen annealed at 650°C shows significantly increased

resistivity due to the formation of Cu-Si compounds which were identified as Cu_3Si and Cu_4Si by subsequent XRD spectra analysis.

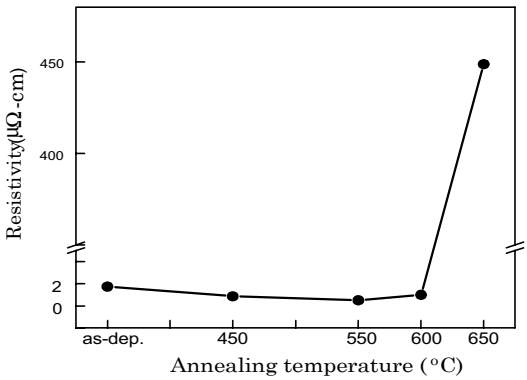


Fig.5. Dependence of the resistivity of the Cu/TaN/Si system on the annealing temperature in H_2 atmosphere.

The adhesion of Cu-film on TaN was examined by a scratch test. Three types of Cu films on TaN/Si substrate were prepared by electroless deposition, sputtering and evaporation methods. Fig.6 shows the variations of acoustic emission with increasing load for Cu films deposited by elecroless deposition, sputtering and evaporation, respectively. As shown in the figure, the critical de-adhesion load taken as the onset of large acoustic emission is higher in order of electroless deposition, evaporation and sputtering from 1.8 to 2.2. Fig.7(a) is the optical micrograph of scratch track showing the overall appearance of scratch film, and Fig.7(b) is the SEM micrograph showing the detailed cracks initiated along the scratch track. Through optical and SEM micrographic observations, cracks were found to occur around 6 N load at which the friction coefficient also began to increase significantly. From the micrograph observation and the variation of friction coefficient, the critical loads required to scribe away the Cu-film were determined to be 5.96 N, 5.80 N, and 5.80 N for electroless deposition, sputtering and evaporation, respectively. Consequently, adhesion of the electroless deposited Cu-film on TaN evaluated by the scratch test was better than those of the sputtered and evaporated Cu-films.

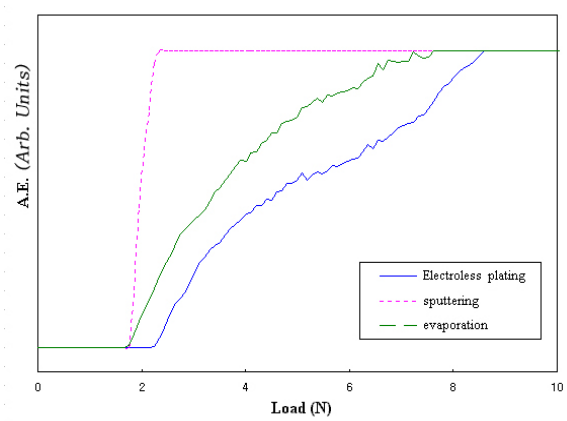


Fig. 6. A.E.(Acoustic Emission) of the scratch test.

(a) (b)

Fig.7. (a) Optical micrograph of the scratch track and (b) SEM micrograph of crack on the scratch track.

Conclusions

The adhesion and thermal properties of the electroless-deposited Cu thin film on the TaN diffusion barrier were investigated. Thermal stability of Cu/TaN/Si system was maintained up to the annealing temperature of 600°C in H_2 atmosphere above which the intermediate compound of Cu-Si was formed through diffusion into the TaN layer. The adhesion of the electroless deposited Cu-film on TaN evaluated by the scratch test was better than those of the sputtered and evaporated Cu-films.

References

1. Muraka, S. P. and Hymes, S. W., "Copper Metallization for ULSI and Beyond", Critical Rev. Solid St. and Mater. Sci., Vol.20, No.3 (1995), pp.87-124.
2. Tao, J., Cheung, N. W. and Hu, C., "Electromigration Characteristics of Copper Interconnects", *IEEE Electron Device Lett.,* Vol.14, No.5 (1993), pp.249-51.
3. Shachamdiamand Y, Dubin V,and Angyal M, "Electroless Copper Deposition for ULSI", *Thin Solid films,* Vol. 262, No. 1-2 (1995), pp.93-103.
4. Vanasupa L, Joo YC, Besser P. R, and Pramanick S, "Texture Analysis of Damascene-fabricated Cu Lines by X-ray Diffraction and Electron Backscatter Diffraction and its Impact on Electromigration Performance", *J. Appl. Phys.* Vol. 85, No.5 (1999), pp.2583-2590.
5. Ryu, C, Kwon, K, Loke, A., Valery M., Dubin, V, Kavari, R, Ray, G and Wong, S, "Electromigaration of Submicron Damascene Copper Interconnects", *Proc. 1998 Sympo. on VLSI Tech.,* Honolulu, USA, June, 1998, pp.156-157.
6. Oku, T., Kawakami, E., Uekubo, M., Takahiro, K., Yamaguchi, S., and Murakami, M., "Diffusion Barrier Property of TaN between Si and Cu", *J. Appl. Surf. Sci. Vol.99, No.4* (1996), pp.265-272.

Electrical Characterization of Silicided CMOS Devices for Embedded DRAM and Logic with Ti and TiN Capping Layers

Jong-Chae Kim, Yeong-Cheol Kim[+], and Hwa-il Seo[*]
Department of Materials Engineering, Korea University of Technology and Education, Chonan, 330-708, Korea
[*]School of Information Technology, Korea University of Technology and Education, Chonan, 330-708, Korea
[+]Email: yckim@kut.ac.kr, Phone: +82-41-560-1326, Fax: +82-41-560-1360

Abstract

Cobalt silicide has been employed to Embedded DRAM (Dynamic Random Access Memory) and Logic (EDL) as a contact material to improve its speed. We have investigated the influences of Ti and TiN capping layers on cobalt-silicided complementary metal-oxide-semiconductor (CMOS) device characteristics. The leakage currents of Ti capped silicided, TiN capped silicided, and non-silicided junctions that experience the full EDL integration with normal DRAM processes for stack cell capacitors are compared. A test pattern with 99 stages of CMOS inverter chain connected in series is also used to evaluate the two capping layer materials by measuring the propagation delay time of the CMOS inverters. TiN capping layer is shown to be superior to Ti capping layer with respect to the current driving capability of pMOSFETs and the resulting propagation delay time of CMOSFETs.

Introduction

Titanium silicide($TiSi_2$) and cobalt silicide($CoSi_2$) have been employed as gate electrode materials in silicon-based very large-scale integration (VLSI) circuits, as a consequence of their low electrical resistivities and good processing compatibilities. [1,2] $TiSi_2$, however, suffers from high electrical resistivity for sub-quarter micron generations due to the difficulty of phase transition from high resistivity C-49 phase to low resistivity C-54 phase during the second rapid thermal annealing (RTA) of the two-step RTA process. [3] Meanwhile, since $CoSi_2$ could maintain its low resistivity on much narrower lines, it has been employed as a gate electrode material by several companies targeting for their sub-quarter micron technology generations. [4]

Recently, needs for Embedded DRAM (Dynamic Random Access Memory) and Logic (EDL) technology have been rapidly increasing in an effort to merge DRAM cell arrays and logic circuits in a single chip for the advantages of lower power consumption and higher performance. [5,6] We have empolyed cobalt silicide as a source/drain contact material to maintain high-speed logic devices in the EDL technology. [7] Cobalt silicidation has been conducted under TiN or Ti capping layer to prevent the oxidation of cobalt layer during the silicidation process. [8,9] Especially, epitaxial cobalt silicidation has been studied by inserting titanium, silicon dioxide, or silicon-germanium alloy between cobalt and silicon to retard the reaction between the two materials, resulting in excellent thermal stability of cobalt disilicide upon post annealing. [10,11,12] In addition, TiN capping layer has been employed to reduce an unfavored reaction of cobalt and silicon with oxygen from air, and Ti capping layer to retard also the reaction between cobalt and silicon, resulting in a high quality polycrystalline cobalt disilicide. [13]

This work presents the effects of Ti and TiN capping layers on cobalt-silicided CMOS device characteristics under a full integration of EDL. The TiN capping layer is shown to be superior to the Ti capping layer with respect to the current driving capability of pMOSFETs and propagation delay time of CMOSFETs.

Experimental

The substrates used in this study were p-type Si (001) wafers with electrical resistivity of 9-12 ohm cm. Phosphorus (P) and boron (B) were ion-implanted to form n and p-well in the substrate after Shallow Trench Isolation (STI). Appropriate n and p-type dopant ion implantations for threshold voltage control of MOSFET devices were conducted in n and p-channel region, respectively. After gate etching process, reoxidation and Lightly Doped Drain (LDD) ion implantation were performed.

Rapid Thermal Annealing (RTA) process was performed to activate the implanted dopants. The samples were dipped in a diluted HF solution prior to cobalt (Co) film deposition to remove native oxide. Co film was sputter deposited without breaking vacuum in a DC magnetron sputtering system.[13] To investigate the effects of capping materials on the full integrated EDL with cobalt silicide in source/drain region, Ti and TiN capping materials were sputter deposited on the Co films, respectively. Subsequent RTA was carried out at 600℃ for 60 sec in an N_2 ambient (first RTA). Unreacted metals were then removed in metal etchant solutions. Additional annealing was performed at 750℃ for 30 sec to form low resistivity $CoSi_2$ (second RTA). In the case of DRAM part, a stack capacitor structure based on NO dielectric was used. Subsequently, BPSG layer was deposited and subjected to a reflow process for planarization for 60 min at 850℃.

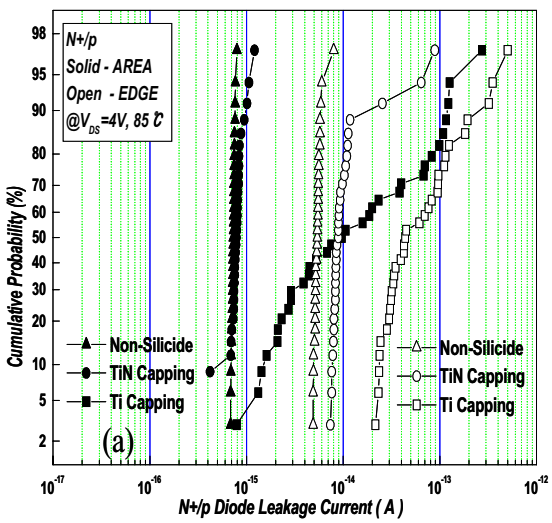
Results and Discussion

The leakage currents of TiN capped silicided, Ti capped silicided, and non-silicided junctions that experience the full EDL integration with normal DRAM processes for stack cell capacitors were compared in Fig. 1. The junction leakage data were obtained from two types of patterns (area-dominant and edge-dominant patterns), and represented by solid and open symbols, respectively. The leakage currents were measured by applying 4 V of V_{DS} to drain and source at 85℃. The junction leakage level of TiN capped silicided junctions was comparable to that of non-silicided junctions. In the case of Ti capping layers, however, larger leakage currents as well as wider leakage current distributions were observed. TEM observation revealed that the interface morphology between

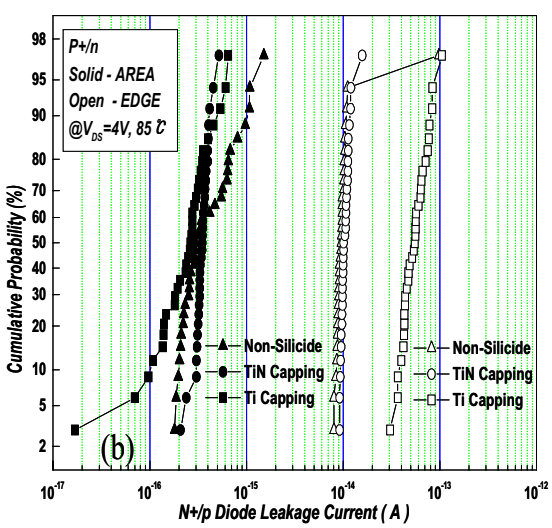
$CoSi_2$ and Si with Ti capping was rougher than that with TiN capping. [14]

In Fig. 2, the I_D-V_D characteristics of nMOSFET and pMOSFET devices that have experienced the full EDL integration were shown. The width of MOSFETs was fixed at 15 ㎛.. In the case of nMOSFETs, no difference between TiN and Ti capping layers was shown. On the contrary, a remarkable difference between TiN and Ti capping layers was exhibited in pMOSFETs. The drain current of pMOSFET with Ti capping layer was greatly reduced compared with those with non-silicide and TiN capping.

The effect of degraded pMOSFETs on the propagation delay time (t_{pd}) of CMOS inverter chain (L_g = 0.35 ㎛) was investigated. A test pattern with 99 stages of CMOS inverter chain connected in series was used to measure the propagation delay time of the CMOS inverter. As shown in Fig. 3, a good t_{pd} value of 71 picosec/stage was obtained at the inverter chain with TiN capping layer, while that of the inverter chain with Ti capping layer was 91 picosec/stage. For reference, the t_{pd} value of non-silicided CMOS inverter chain was measured as shown in Fig. 3(a), and was 167 picosec/stage.

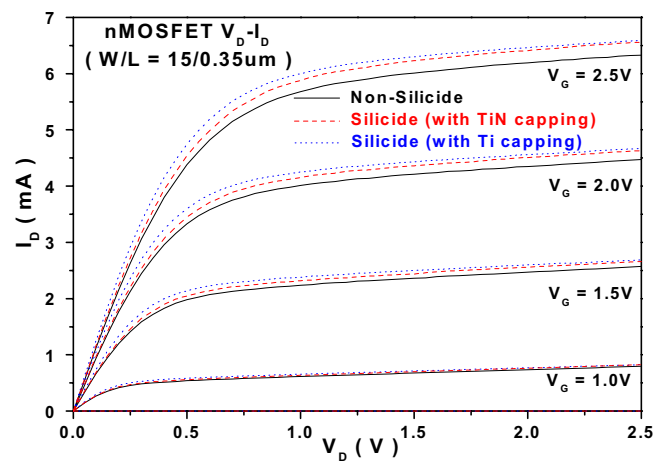


(a)

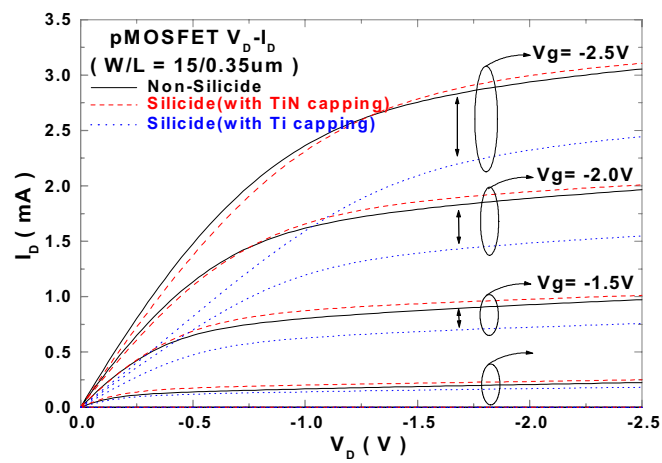


(b)

Fig. 1. Cumulative probability of junction leakage currents in (a) N+/p and (b) P+/n junction diodes at 4V and 85℃ after the full EDL processes.

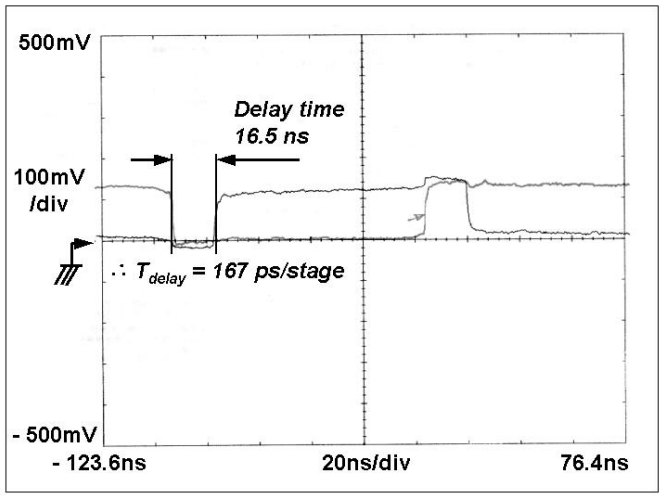


(a)

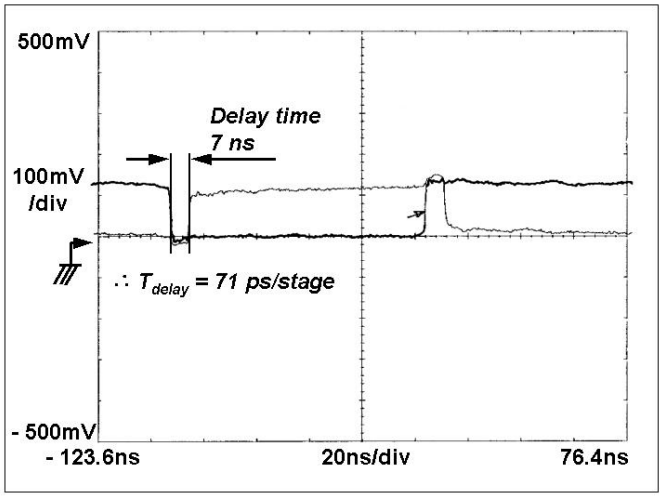


(b)

Fig. 2. I_D-V_D characteristics of (a) nMOSFET and (b) pMOSFET.



(a)



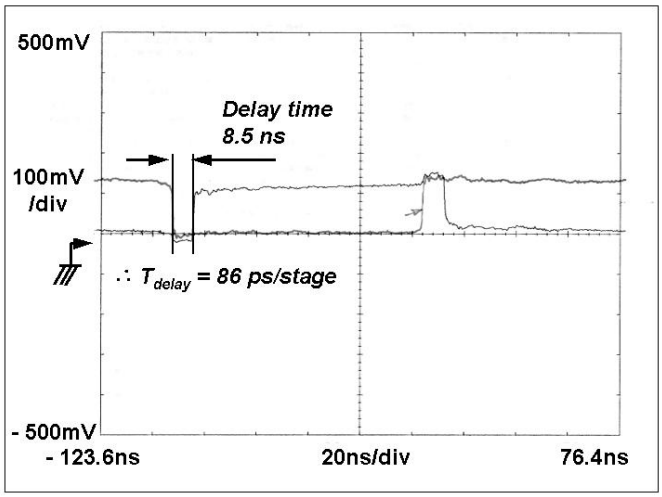


Fig. 3. Propagation delay time of CMOS inverter chains with (a) non-silicided, (b) TiN capped silicided, and (c) Ti capped silicided source/drain regions.

Conclusion

We have investigated the influences of TiN and Ti capping layers on cobalt-silicided CMOS device characteristics. After the full integration of EDL including DRAM processes, the TiN capping layer was shown to be superior to the Ti capping layer with respect to the current driving capability of pMOSFETs and the resulting propagation delay time of CMOSFETs.

References

1. Maex, K., "Silicides for Integrated Circuits: $TiSi_2$ and $CoSi_2$," *Mat. Sci. Eng. Rep.,* R11 (1993) pp. 53-153.
2. Colgan, E. G. *et al*, "Formation and Stability of Silicides on Polycrystalline Silicon," *Mat. Sci. Eng. Rep.,* R16, 43-96 (1996).
3. Y-C. Kim, "Diffusion-accompanied Phase Transformation of $TiSi_2$ Film Confined in Sub-micron Area," *J. Kor. Ceram. Soc.*, Vol. 7, No. 2 (2001) pp. 70-73.
4. Bae, J-U. *et al*, "Improvement of $CoSi_2$ Stability on Fine Grain Sized Poly-Si Using Nitrogen Implantation Through Co Monosilicide and Its Effects on 0.18μm Dual Gate CMOS," *Tech. Dig. Int. Symp. VLSI Tech.* (1999) pp. 53-54.
5. Kim, J. C. *et al*, "Co-silicide Junction Leakage and Device Characteristics in Embedded DRAM with Stack Capacitor Structure," *ESSDERC99 Proc.* (1999) pp. 228-231.
6. Ishiuchi, H. *et al*, "Embedded DRAM Technologies," *IEDM Tech. Dig.* (1997) pp. 33-36.
7. Kim, J. C. *et al*, "Effect of Dopants on Cobalt Silicidation Behavior at Metal-oxide-semiconductor Field-effect Transistor Sidewall Spacer Edge," *To appear in J. Kor. Ceram. Soc.*, Vol. 10 (2001).
8. Wang, Q. F. *et al*, "New $CoSi_2$ Salicide Technology for 0.1 ㎛ Processes and Below," *Symp. on VLSI Tech.* (1995) pp. 17-19.
9. Goto, K. *et al*, "Optimization of Salicide Processes for 0.1 ㎛ CMOS Device," *Symp. on VLSI Tech.* (1994) pp. 119-120.
10. Kim, G. B. *et al*, "Control of Co Flux Through Ternary Compound for the Formation of Epitaxial $CoSi_2$ Using Co/Ti/Si System," *Appl. Phys. Lett.*, Vol. 69, (1996) pp. 3498-3500.
11. Tung, R. T, "Oxide Mediated Epitaxy of $CoSi_2$ on Silicon," *Appl. Phys. Lett.*, Vol. 68, (1996) pp. 3461-3463.
12. Donaton, R. A. *et al,* "Co Silicide Formation on SiGeC/Si and SiGe/Si Layers," *Appl. Phys. Lett.*, Vol. 70 (1997) pp. 1266-1268.
13. Sohn, D. K. *et al*, "Formation of CoTi Barrier and Increased Thermal Stability of $CoSi_2$ Film in Ti Capped Co/Si (100) System," *Appl. Phys. Lett.*, Vol. 73 (1998) pp. 2302-2304.
14. J. C. Kim *et al*, "Effects of Ti and TiN Capping Layers on Cobalt-silicided MOS Device Characteristics in Embedded DRAM and Logic," *J. Kor. Ceram. Soc.*, Vol. 38, No. 9 (2001) pp. 782-786.